H JONES

Instruction manual

DATA I/O

Programming systems for tomorrow...today

PROM PROGRAMMER
Program Card Set
909/919-1286-1

REV J OCT 81

025-1286-1

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SECTION 1
SPECIFICATIONS

1.1 INTRODUCTION

Data I/O Program Card Sets configure the programmer for the requirements of particular devices. This card set, used with the appropriate socket adapter, will program and read the devices listed in Table 1-1. New applications are developed frequently; therefore, consult the most recent Data I/O Comparison Chart of Programmable Devices to supplement Table 1-1.

Table 1-1. Applications of the Program Card Set

Array Size and Technology	PROM Part Number	Programmed Logic Level	Pinout	Socket Adapter
ADVANCED MICRO DEVICES				
32x8 FL	27S18/29750A	VOH OC	16 PIN	1407-1
32x8 FL	27S19/29751A	VOH TS	16 PIN	1407-1
256x4 FL	27S20/29760A	VOH OC	16 PIN	1408-1
256x4 FL	27S21/29761A	VOH TS	16 PIN	1408-1
512x4 FL	27S12/29770	VOH OC	16 PIN	1408-2
512x4 FL	27S13/29771	VOH TS	16 PIN	1408-2
512x8 FL	27S15	VOH TS	24 PIN	1411-1
512x8 FL	27S24	VOH OC	24 PIN	1617
512x8 FL	27S25	VOH TS	24 PIN	1617
512x8 FL	27S26/29774	VOH OC	22 PIN	1412-2
512x8 FL	27S27/29775	VOH TS	22 PIN	1412-2
512x8 FL	27S28	VOH OC	20 PIN	1413
512x8 FL	27S29	VOH TS	20 PIN	1413
512x8 FL	27S30	VOH OC	24 PIN	1545
512x8 FL	27S31	VOH TS	24 PIN	1545
1024x4 FL	27S32	VOH OC	18 PIN	1414
1024x4 FL	27S33	VOH TS	18 PIN	1414
1024x8 FL	27S180	VOH OC	24 PIN	1545-2
1024x8 FL	27S181	VOH TS	24 PIN	1545-2
2048x4 FL	27S184	VOH OC	18 PIN	1616
2048x4 FL	27S185	VOH TS	18 PIN	1616

The Program Card Set includes the parts listed in Figure 1-1. The analog card produces the correct voltages in the proper waveforms for the device to be programmed or read. The digital card controls the sequences and shapes of these waveforms.

A Program Card Set for use in a System 17 or 19 Programmer is included in a Programming Pak and designated by a 919- part number. See Figure 1-1 a). A card set shipped alone, for use in a Model 1-5, 7 or 9 Programmer, bears a 909-part number. See Figure 1-1 b).

1.2 CALIBRATOR PROGRAM ADAPTER

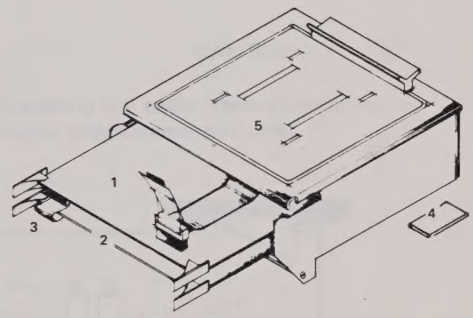
The card set includes a Calibrator Program Adapter which mates with the Data I/O Universal Calibrator (P/N 910-1071). The PROMs on the adapter deliver the control signals to the analog card.

Using the calibrator and following the calibration procedure in Section 4 of this manual, Data I/O customers can be sure the Program Card Set remains within voltage and timing tolerances for effective programming.

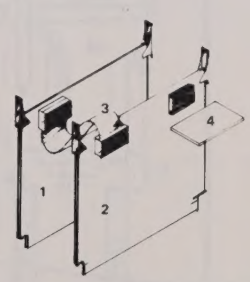
1.3 CALIBRATION REQUIREMENTS

The need for calibration varies with the amount of use; calibration is recommended every ninety days of regular use or if programming yields fall below manufacturer's recommended minimums.

Complete calibration must be performed with a programmer that has an address and data display. Card sets for use in a Model 7 or System 17 may be properly calibrated using another Data I/O programmer. Alternately, Data I/O provides calibration service at regional Service Centers.



a) Programming Pak for System 17 and 19 Programmers



b) Program Card Set for Model 1-9 Programmers

1. DIGITAL CARD	701-1225
2. ANALOG CARD	701-1286-1
3. INTERCONNECT CABLE	709-1608
4. CALIB. PROGRAM ADAPTER	910-1286-1
5. PROGRAMMING PAK CARRIER	940-0919

Figure 1-1. Parts included in the a) Programming Pak b) Program Card Set

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SECTION 2
INSTALLATION

2.1 DIGITAL CARD JUMPERS

Figure 2-1 shows the customer-selectable-jumper locations on the digital card. Refer to Table 2-1 to check the jumper positions. If a jumper change is ever made, be sure to replace the jumpers in the normal position before using the card set for programming.

Table 2-1. Customer-Selectable Digital Card Jumpers

JUMPER	FUNCTION	NORMAL POSITION	COMMENTS
JP7	Reject	C	See the timing diagram to determine the number of reject pulses selected.
JP10	Word Limit	2048	Selection defaults to socket adapter

2.2 CARD SET INSERTION

When changing card sets in Model 1-9 Programmers, turn power OFF.

Power may remain ON when changing Programming Paks in System 17 or 19 Programmers. In this way, data may be retained in RAM during the operation.

2.2.1 MODELS 1-5

Refer to Figure 2-2.

Remove the top cover from the programmer. Each card in the card cage has color-coded extractors which correspond to the colors of the card guides. Install the analog card in the white/white position in the card cage. Install the digital card in the front brown/orange position. Components of both cards must face forward in Model 3 and 5 Programmers and to the right in Model 1 and 2 Programmers. Insert the cable into the socket receptacle, route it over the card cage, and attach it to J2 on the analog card. Be sure the cable is oriented correctly: the red stripe must align with the connector dot.

CAUTION

Installing the cable backwards could cause programmer damage.

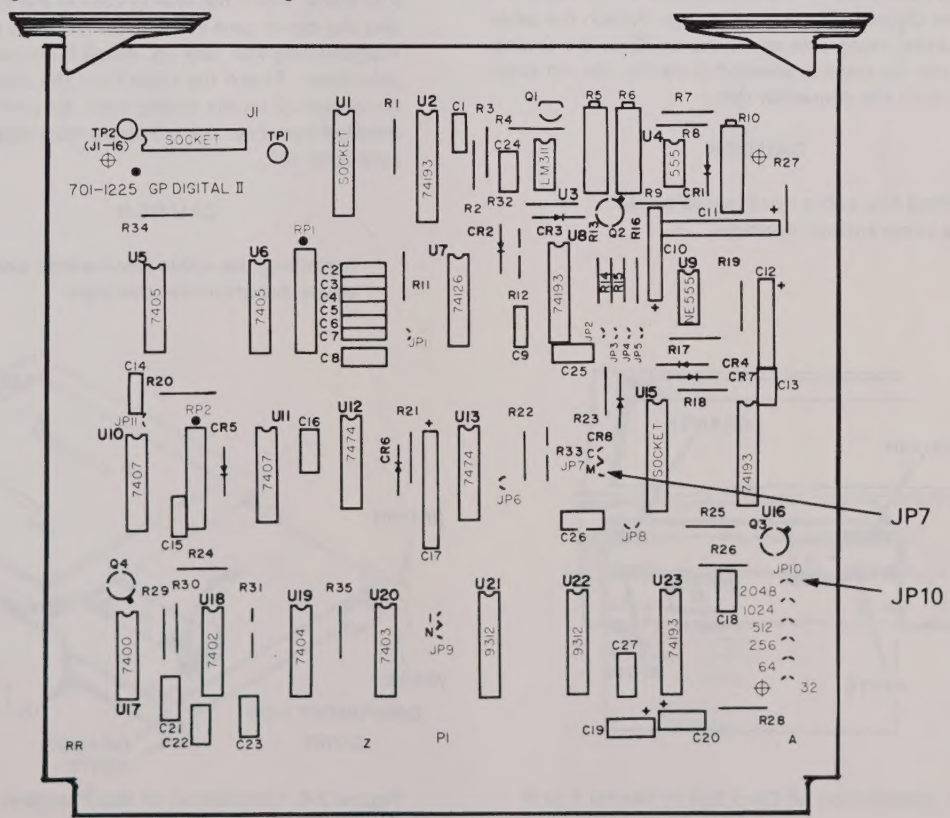


Figure 2-1. Digital Card Jumper Locations

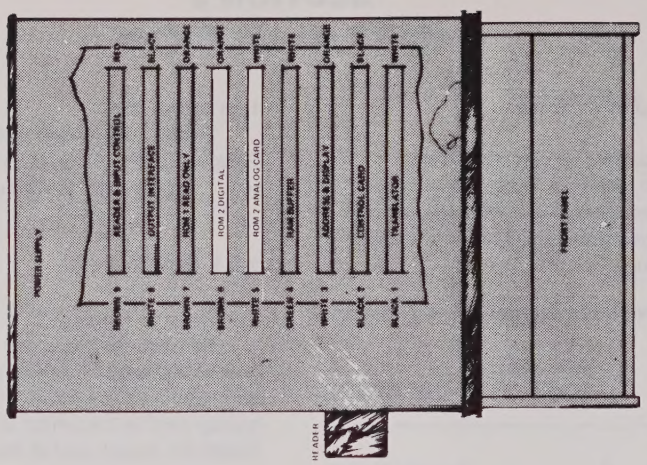


Figure 2-2. Installation of Card Set in Model 3 or 5

2.2.2 MODELS 7 AND 9

Refer to Figure 2-3.

The card set access door is located at the front of the programmer on the right-hand side. Open the door from the bottom to expose the card slots. The card guides are colored white/white and brown/orange to correspond with the extractor tabs on the cards. Insert both cards component-side-down — the analog card in the white/white slot and the digital in the brown/orange. Attach the cable from the socket receptacle to connector J2 on the analog card. Be sure the cable is oriented correctly: the red stripe must align with the connector dot.

CAUTION

Installing the cable backwards could cause programmer damage.

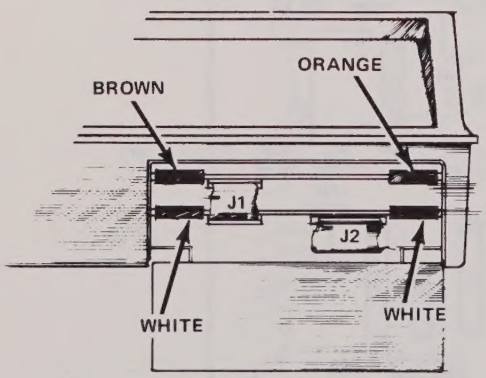


Figure 2-3. Installation of Card Set in Model 7 or 9

2.2.3 SYSTEMS 17 AND 19

Refer to Figure 2-4.

The card set should normally remain in the Programming Pak frame. Install the Programming Pak into the programmer by sliding it into the opening and lowering into position. Press gently on the handle to insure connector mating.

If the card set needs to be installed in its Programming Pak frame, insert the analog card in the white/white slot and the digital card in the brown/orange slot. With the Programming Pak face up, install both cards component-side-down. Attach the cable from the socket receptacle to connector J2 on the analog card. Be sure the cable is oriented correctly: the red stripe must align with the connector dot.

CAUTION

Installing the cable backwards could cause programmer damage.

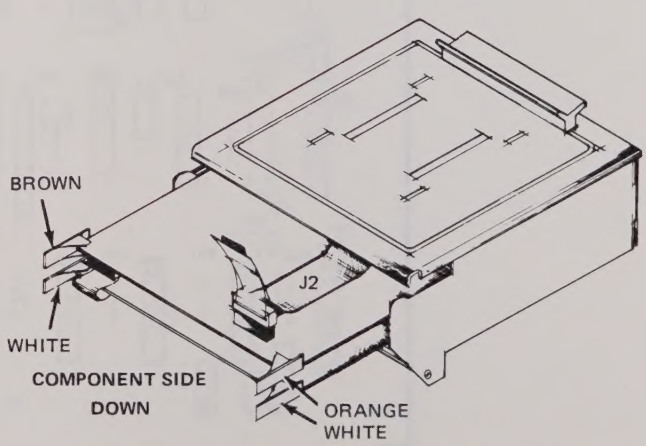


Figure 2-4. Installation of the Program Card Set in the Programming Pak

SECTION 3
OPERATION

The Program Card Set provides the link between the device in the socket adapter and the programmer's memory and control electronics. Its functions are directly controlled by the programmer. Complete instructions for operations using the card set are in the programmer instruction manual.

SECTION 4
CALIBRATION

4.1 INTRODUCTION

Calibration includes checks of power supply levels, steady-state tests of critical programming parameters, and verification of resistively loaded programming waveforms. The need for calibration varies with the amount of use, but calibration is suggested at least every ninety days. For calibration by the customer, the procedure in this section should be followed in sequence.

NOTE

If any adjustment is necessary, complete the entire calibration procedure.

4.2 TEST SET-UP

The following equipment is required to perform a calibration:

a. Data I/O Universal Calibrator, P/N 910-1071

b. Calibration Extender:

Models 1-5	P/N 910-1136
Model 9	P/N 910-1074
System 19	P/N 910-1521

c. Digital voltmeter (DVM) — Fluke Model 8000A or equivalent.

d. A potentiometer adjustment tool

e. Dual-trace oscilloscope — Tektronix 465 or equivalent

f. A jumper wire approximately 12 inches in length

g. Data I/O interconnection cables:

Models 1-5	P/N 709-1613
Model 9	P/N 709-2608, 709-1613
System 19	P/N 709-2612, 709-1613

h. Calibrator Program Adapter

To prepare for calibration of the programmer power supplies and the Program Card Set, remove the card set from the programmer and connect the Universal Calibrator according to the following instructions:

4.2.1 MODELS 1-5

Refer to Figure 4-1.

a. Make sure the programmer power is OFF.

b. Remove the cover from the programmer and remove the Program Card Set from the card cage.

c. Disconnect the 16-conductor cable from J1 on the digital card; disconnect the 26-conductor cable from J2 on the analog card.

CAUTION

Connector pins are fragile; use a suitable tool, such as a small screwdriver, when removing cables from their connectors.

d. Install the Extender Card, P/N 910-1136, (with the Universal Calibrator attached) into the programmer's analog card position (white/white). Be sure that the edge of the Extender Card is securely seated. Reinstall the digital card in the digital card position (brown/orange) in the programmer card cage.

e. Connect the 16-conductor cable from J1 on the analog card to J1 on the Universal Calibrator. Connect the 26-conductor cable from J2 on the analog card to J2 on the Universal Calibrator. Be sure the cables are oriented correctly: the red stripes must align with the connector dots.

f. Plug the Calibrator Program Adapter into the Program Adapter socket on the Universal Calibrator.

CAUTION

Be sure the Calibrator Program Adapter part number corresponds to the part number of the Program Card Set.

g. Connect the DVM ground lead to the GND test point on the Universal Calibrator.

h. Turn the programmer power ON. Prepare the programmer for calibration using the following key sequence:

RESET
ROM2 — ROM2
MANUAL
PROGRAM
START

Figure 4-1. Set-up of Models 1-5 for DC Calibration.

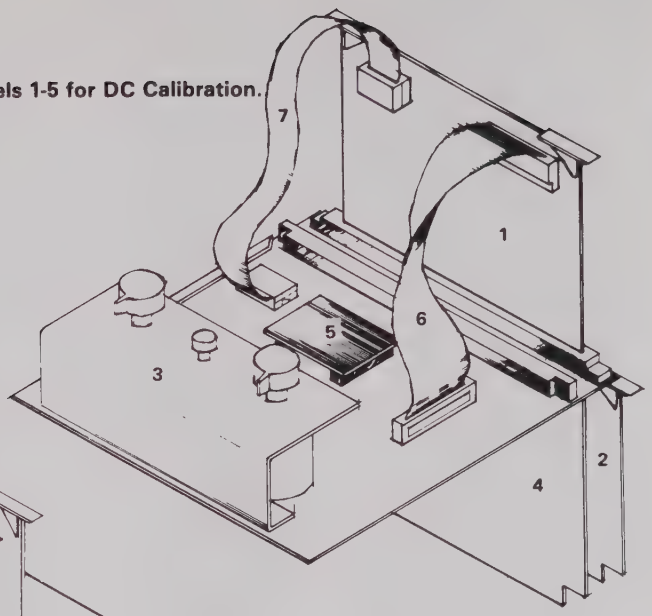
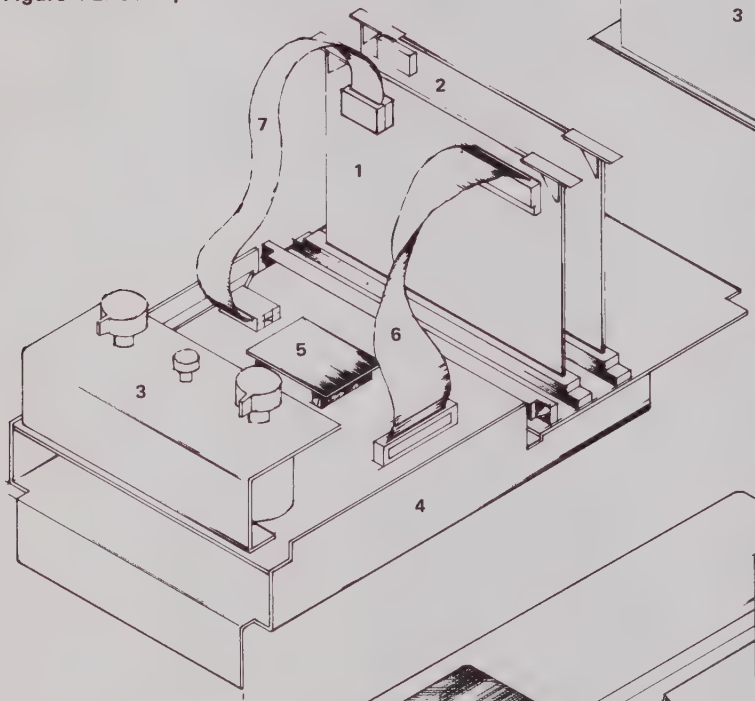
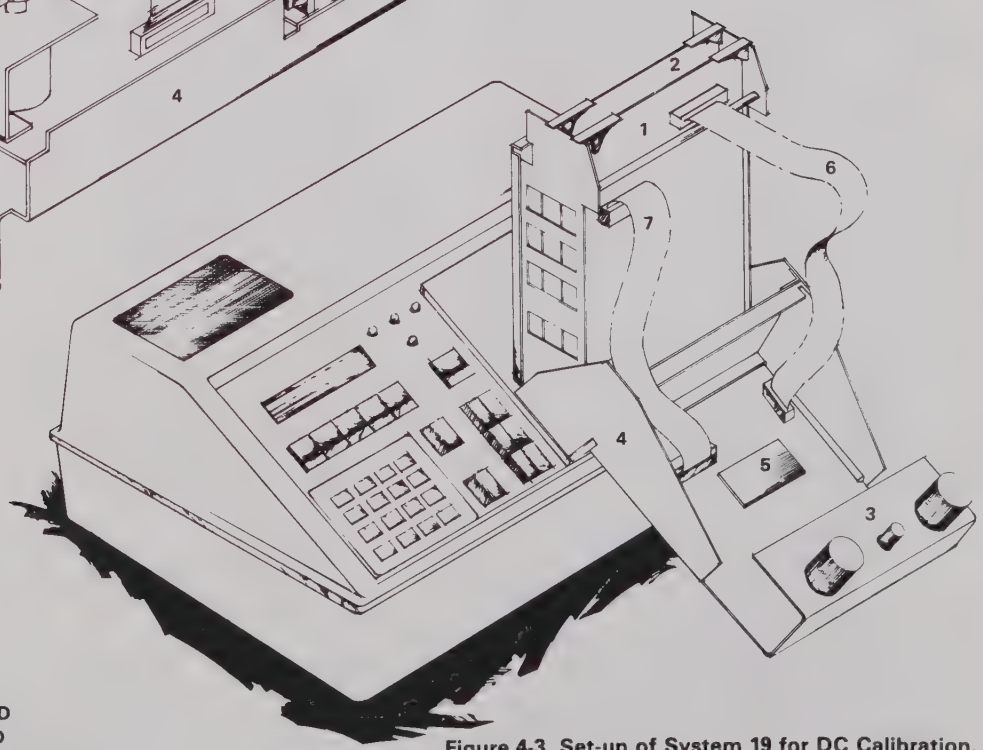


Figure 4-2. Set-up of Model 9 for DC Calibration.





1. ANALOG CARD
2. DIGITAL CARD
3. UNIVERSAL CALIBRATOR
4. CALIBRATION EXTENDER
5. CALIBRATOR PROGRAM ADAPTER
6. 26-CONDUCTOR CABLE
7. 16-CONDUCTOR CABLE

Figure 4-3. Set-up of System 19 for DC Calibration.

4.2.2 MODEL 9

Refer to Figure 4-2.

a. Make sure the programmer power is OFF.

b. Open the Program Card Set access door from the bottom. Remove the Program Card Set.

CAUTION

Connector pins are fragile; use a suitable tool, such as a small screwdriver, when removing cables from their connectors.

c. Disconnect the 16-conductor cable from J1 on the digital card; disconnect the 26-conductor cable from J2 on the analog card.

d. Install the Extender Card, P/N 910-1074, (with the Universal Calibrator attached) into the programmer's digital card position (brown/orange). Be sure that the edge of the Extender Card is securely seated. Install the Digital and Analog cards into the 1074 calibration extender according to Figure 4-2.

e. Connect the 16-conductor cable from J1 on the analog card to J1 on the Universal Calibrator. Connect the 26-conductor cable from J2 on the analog card to J2 on the Universal Calibrator. Be sure the cables are oriented correctly: the red stripes must align with the connector dots.

f. Plug the Calibrator Program Adapter into the Program Adapter socket on the Universal Calibrator.

CAUTION

Be sure the Calibrator Program Adapter part number corresponds to the part number of the Program Card Set.

g. Connect the DVM ground lead to the GND test point on the Universal Calibrator.

h. Turn the programmer power ON. Prepare the programmer for calibration using the following key sequence:

KEYBOARD
EXECUTE

NORMAL/INVERT switch to INVERT

4.2.3 SYSTEM 19

Refer to Figure 4-3.

a. Make sure the programmer power is OFF.

b. Remove the Programming Pak from the programmer.

c. Insert the Calibration Extender, P/N 910-1521, in the same way as the Programming Pak, being sure to seat it properly in the programmer's mating connector.

d. With the handle of the Programming Pak down, connect the 64-pin connectors of the Programming Pak and Calibration Extender. Be sure the connectors mate securely.

e. Slide the Universal Calibrator securely into the card slots at the front of the Calibration Extender.

f. Connect the 26-conductor cable from J2 of the analog card to J2 of the Universal Calibrator, making sure to align the red stripe with the connector dot.

g. Disconnect the 16-conductor cable from J1 on the digital card and route it to J1 on the Universal Calibrator, making sure to align the red stripe with the connector dot.

h. Plug the Calibrator Program Adapter into the Program Adapter slot on the Universal Calibrator.

CAUTION

Be sure the Calibrator Program Adapter part number corresponds to the part number of the Programming Pak.

i. Connect the DVM ground lead to GND test point on the Universal Calibrator.

j. Turn the programmer power ON. Prepare the programmer for calibration using the following key sequence:

SELECT
C1 (calibrate ON)
START

k. Press:

KEYBD
ENTER

The TEST light comes ON and remains ON throughout calibration.

NOTE

To exit calibration, press:
SELECT
CØ (calibrate OFF)
START
(Test light goes OFF.)

l. Press START.

4.3 PROCEDURES FOR CALIBRATION

The Calibration Chart, between pages 4-4 and 4-5, gives the steps for complete DC calibration. It is to be used only with the Calibrator Program Adapter specified in the title block of the chart.

The first five steps on the Calibration Chart cover the level checks of the programmer power supplies. If any adjustment is necessary in these steps, refer to the Programmer Manual. The remaining steps provide information for calibration of the Program Card Set.

- The PROGRAMMER WORD COUNT column is divided into three portions: DEC (Decimal), HEX (Hexadecimal), and OCT (Octal). When performing each step, set the address (word count) corresponding to the address number base of the programmer in use. For instance, with a programmer having a hexadecimal address readout, ignore the DEC and OCT columns.

CAUTION

DO NOT leave Word Count (address) advanced beyond 000 for extended periods. Static conditions created by the Universal Calibrator may cause thermal damage to components if the programmer is left unattended with advanced word count.

- The TEST DESCRIPTION column specifies the function to be checked in each step. In most cases, the steps simply require a DVM reading to insure that a level is within tolerance. Some steps, labeled Adjustment Steps, give a nominal (NOM) value and prescribe adjustment to that value if the level is out of the MIN-MAX range.

- The ADJUSTMENT column calls out potentiometer designations. The first four entries in the ADJ column refer to power supply potentiometers located on the power supply board of the programmer. The remaining entries in the ADJ column refer to potentiometers on the analog card. Refer to Figure 4-4 for locations of the potentiometers.

- The SWITCH POSITIONS column gives the switch settings for S2 and S3 on the Universal Calibrator. S2 is the load-select switch; S3 is the line-select switch. Each step on the Calibration Chart may require changing of switch positions. With the proper S2 and S3 positions selected, press S1 to make an accurate reading, and keep the switch depressed only long enough to complete the step.

CAUTION

DO NOT keep S1 depressed for extended periods. Certain measurements induce high programmer current levels. Extended high-current operation (S1 depressed) may damage sensitive electronic components.

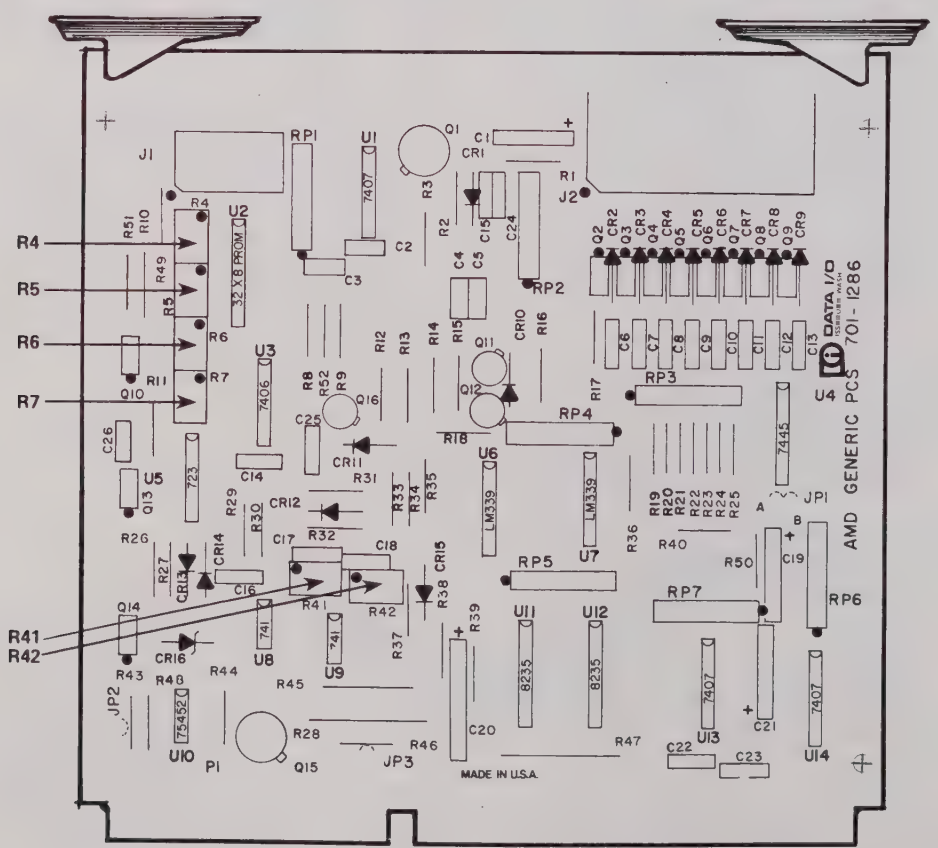


Figure 4-4. Analog Card Adjustment Locations

- The TEST POINT column gives test point locations for the DVM probe. Most test points are located on the Universal Calibrator; some points are located on the program card. For instance, if a test point is designated as U6 P8, the DVM probe should be placed on pin 8 of integrated circuit U6 on the card indicated in the COMMENTS column.

- The LIMITS column is divided into three portions: MIN (minimum), NOM (nominal), and MAX (maximum). The values given are in volts and indicate the range into which a given DVM reading should fall. If a reading is within the limits, no adjustment is required and the programmer (or Program Card Set) passes a particular test. If a reading falls outside of the given limits, or if it cannot be adjusted to fall within the limits (in adjustment steps), the card is nonfunctional and should not be used for programming.

- The COMMENTS column on the right side of the chart provides information for certain calibration steps including call-outs of programmer operations required in some steps. The programmer provides signals to the card set on the Address bus, the Data Input bus, the START/STOP line and the FWD/REV line. The card set provides signals to the programmer on the RESET line, the VOL/VOH select line and the Data Output bus. In the course of calibration, the programmer is used to observe or set the following conditions:

- State of the START/STOP line
- State of the FWD/REV line
- Data on the DO bus
- Data on the DI bus

Key sequences for observing these conditions are given in the following paragraphs (4.3.1 — 4.3.5). Follow the tests on the Calibration Chart step-by-step, and refer to paragraphs 4.3.1 — 4.3.5 as necessary.

MODEL 9 USERS NOTE

Some of the following operations are performed differently on Model 9's with different revisions of software. Perform the following test to determine whether to refer to steps for Revision "A" software or to steps for Revision "B" or later software.

1. *Turn power OFF.*
2. *Observe the LOAD indicator while turning power ON.*
3. *If the LOAD indicator remains ON, refer to key sequences for Revision "B" or later software.*
4. *If the LOAD indicator turns OFF, refer to key sequences for Revision "A" software.*

4.3.1 CHECK THE STATE OF THE START/STOP LINE

For steps that require confirmation of the state of the START/STOP line, perform the check as follows. To continue testing after confirming a STOP condition, START the programmer according to paragraph 4.3.2.

Models 1, 2, 3 and 5:	Observe the START and STOP indicators.
Model 9:	Press the PROM key and observe the data display. The programmer is in STOP if the display is blank; in START if the display shows data.
System 19:	Observe the START light. If the START light is on, the programmer is in START.

4.3.2 SET THE STATE OF THE START/STOP LINE

Models 1, 2, 3 and 5:	Press the START/STOP key.
Model 9:	a. Press KEYBOARD to stop.
	b. Press EXECUTE to start.
System 19:	a. To set the programmer in START, press KEYBD, ENTER and START.
	b. To set programmer in STOP, press KEYBD.

4.3.3 SET THE STATE OF THE FWD/REV LINE

To set the programmer in FORWARD or in REVERSE:

Models 1, 2, 3 and 5:	Press the FWD key or the REV key.
Model 9:	See MODEL 9 USERS NOTE, paragraph 4.3, to determine the right revision letter.
Revision "A" Software:	Halt the programmer in FWD and in REV by entering data at an address and causing a mis-verify:
	a. Ground J1-16 on the analog card.
	b. Press LOAD.
	c. Press EXECUTE.
	d. Press KEYBOARD.
	e. Key in data — Ø hex — at address ØØ1.
	f. Press VERIFY.
	g. Press EXECUTE. The programmer will mis-verify

Calibration Chart

DATA I/O
Programming systems for tomorrow...today

CALIBRATION CHART 017-1286-1 | PROGRAM CARD 909-1286-1
FIXTURE 702-1071 | MANUFACTURER A.M.D.
PAGE 1 OF 3 | PROGRAM ADAPTER 910-1286-1 | PROM GENERIC FAMILY

DATE	REV	REVISION RECORD	DR	CK
5-78	D	CN #2230	KL	KJ
6-78	E	CN #2308	KJ	RT
7-78	F	CN #2332	KJ	RT
4-79	—	CN #2565	FS	
5-27-80	G	ECN #3558	KJB	

CAL ADAPT HEX DATA (POS. LOGIC) LOCATION U2	U1	TEST DESCRIPTION	STEP NO.	PROGRAMMER WORD COUNT DEC	HEX	OCT	SWITCH POSITIONS S2	S3	MEASUREMENT TEST PT.	ADJ.	LIMITS MIN	NOM	MAX	COMMENTS
44	0A	+24	1-1	000	00	000			+24	R26	23.5	24.0	24.5	Adjustments are located on the power supply board. See programmer manual.
44	0A	POWER +48	1-2	000	00	000			+48	R24	49.4	49.7	49.8	
44	0A	SUPPLIES +5	1-3	000	00	000			+5	R18	5.05	5.1	5.15	
44	0A	-9	1-4	000	00	000			-9	R40	-9.2	-9.0	-8.8	
44	0A	PROGRAMMABLE SUPPLY	1-5	000	00	000			PROG V		27.0		29.0	
44	0A	VCC VERIFY VL	2-0	000	00	000	5	1	TP3	R6	4.00	4.25	4.50	*Adjustment Step.*
44	0E	VCC VERIFY VH	2-1	001	01	001	5	1	TP3	R5	4.75	5.00	5.25	*Adjustment Step.*
44	06	VCC READ	2-2	002	02	002	5	1	TP3	R4	4.75	5.00	5.25	*Adjustment Step.*
54	03	VCC PROGRAM (1)	2-3	003	03	003	5	1	TP3	R7	5.00	5.25	5.50	*Adjustment Step.*
54	03	VCC CURRENT ICC	2-4	003	03	003	6	1	TP3		5.0		8.0	
54	03	VCC KILL	2-5	003	03	003	5	1	TP3		0.0		0.4	Set programmer in STOP.
54	03	VERIFY REFERENCE	3-1	003	03	003			U7 P8		1.6		1.8	Test point located on analog card.
54	03	VERIFY LOAD IN	3-2	003	03	003	3	8	TP3		1.8		2.6	
54	04	VERIFY LOAD OUT	3-3	004	04	004	7	8	TP3		0.0		1.0	
54	04	$\overline{CE}$ PROGRAM (2)	4-1	004	04	004	3	5	TP3	R41	14.5	15.0	15.5	*Adjustment Step.*
54	0E	$\overline{CE}$ DISABLE	4-2	005	05	005	7	5	TP3		3.5		4.5	
54	0F	$\overline{CE}$ VERIFY	4-3	006	06	006	7	5	TP3		0.0		0.4	
64	0F	CP LOW LEVEL (6)	4-4	006	06	006	7	6	TP3		0.0		0.4	
64	16	CP HIGH LEVEL	4-5	007	07	007	7	6	TP3		4.8		5.15	
64	E4	BIT 8 PROGRAM V OUT SET	5-1	008	08	010	5	8	TP3	R42	19.5	20.0	20.5	*Adjustment Step.*
64	C4	BIT 8 NO PROGRAM	5-2	009	09	011	7	8	TP3		0.0		1.0	
64	C4	BIT 7 PROGRAM	5-3	009	09	011	5	9	TP3		19.5		20.5	
64	A4	BIT 7 NO PROGRAM	5-4	010	0A	012	7	9	TP3		0.0		1.0	
64	A4	BIT 6 PROGRAM	5-5	010	0A	012	5	10	TP3		19.5		20.5	
64	84	BIT 6 NO PROGRAM	5-6	011	0B	013	7	10	TP3		0.0		1.0	
64	84	BIT 5 PROGRAM	5-7	011	0B	013	5	11	TP3		19.5		20.5	
64	64	BIT 5 NO PROGRAM	5-8	012	0C	014	7	11	TP3		0.0		1.0	
64	64	BIT 4 PROGRAM	5-9	012	0C	014	5	12	TP3		19.5		20.5	
64	44	BIT 4 NO PROGRAM	5-10	013	0D	015	7	12	TP3		0.0		1.0	

COMMENTS
- Use paragraphs 4.3.1-4.3.5 for key sequences for COMMENT below.
- Switch S1 must be depressed for accurate readings.
- CAUTION: DO NOT LEAVE S1 DEPRESSED FOR EXTENDED PERIODS.

CAL. ADAPT. HEX DATA (POS. LOGIC) LOCATION U 2	U 1	TEST DESCRIPTION	STEP NO.	PROGRAMMER WORD COUNT DEC	HEX	OCT	SWITCH POSITIONS S2	S3	MEASUREMENT TEST PT.	ADJ.	LIMITS MIN	NOM	MAX
64	44	BIT 3 PROGRAM	5-11	013	0D	015	5	23	TP3		19.5		20.5
64	24	BIT 3 NO PROGRAM	5-12	014	0E	016	7	23	TP3		0.0		1.0
64	24	BIT 2 PROGRAM	5-13	014	0E	016	5	22	TP3		19.5		20.5
64	04	BIT 2 NO PROGRAM (4)	5-14	015	0F	017	7	22	TP3		0.0		1.0
64	04	BIT 1 PROGRAM (3)	5-15	015	0F	017	5	21	TP3		19.5		20.5
64	E4	BIT 1 NO PROGRAM	5-16	016	10	020	7	21	TP3		0.0		1.0
64	E4	BIT CURRENT LIMIT IOP	5-17	016	10	020	6	8	TP3		4.0		6.0
C4	07	BIT 8 COMPARATOR	6-1	017	11	021	5	8					
C4	07	BIT 7 COMPARATOR	6-2	017	11	021	5	9					
C4	07	BIT 6 COMPARATOR	6-3	017	11	021	5	10					
C4	07	BIT 5 COMPARATOR	6-4	017	11	021	5	11					
C4	07	BIT 4 COMPARATOR	6-5	017	11	021	5	12					
C4	07	BIT 3 COMPARATOR	6-6	017	11	021	5	23					
C4	07	BIT 2 COMPARATOR	6-7	017	11	021	5	22					
C4	07	BIT 1 COMPARATOR	6-8	017	11	021	5	21					
C4	07	VOH DETECT											
C4	07	VOL DETECT											
44	07	READ ENABLE	6-11	018	12	022	7	7					
C0	07	GROUND TEST	7-1	019	13	023	8	24	TP3		0.0		0.08
64	A4	ADDRESS TEST A0 VIL (5)	8-1	682	2AA	1252	7	20	TP3		0.0		0.4
64	A4	ADDRESS TEST A1 VIH	8-2	682	2AA	1252	7	19	TP3		4.8		5.15
64	A4	ADDRESS TEST A2 VIL	8-3	682	2AA	1252	7	18	TP3		0.0		0.4
64	A4	ADDRESS TEST A3 VIH	8-4	682	2AA	1252	7	17	TP3		4.8		5.15
64	A4	ADDRESS TEST A4 VIL	8-5	682	2AA	1252	7	16	TP3		0.0		0.4
64	A4	ADDRESS TEST A5 VIH	8-6	682	2AA	1252	7	15	TP3		4.8		5.15
64	A4	ADDRESS TEST A6 VIL	8-7	682	2AA	1252	7	14	TP3		0.0		0.4
64	A4	ADDRESS TEST A7 VIH	8-8	682	2AA	1252	7	13	TP3		4.8		5.15
64	A4	ADDRESS TEST A8 VIL	8-9	682	2AA	1252	7	2	TP3		0.0		0.4
64	A4	ADDRESS TEST A9 VIH	8-10	682	2AA	1252	7	3	TP3		4.8		5.15
64	A4	ADDRESS TEST A10 VIL	8-11	682	2AA	1252	7	4	TP3		0.0		0.4
64	04	ADDRESS TEST A0 VIH	8-12	1365	555	2525	7	20	TP3		4.8		5.15
64	04	ADDRESS TEST A1 VIL	8-13	1365	555	2525	7	19	TP3		0.0		0.4

CALIBRATION CHART 017-1286-1

	MODEL 5	9	19	
Confirm	Bits 1-7 ON	7F	7F	DO Bus
Confirm	Bits 1-6 & 8 ON	BF	BF	DO Bus
Confirm	Bits 1-5 & 7-8 ON	dF	dF	DO Bus
Confirm	Bits 1-4 & 6-8 ON	EF	EF	DO Bus
Confirm	Bits 1-3 & 5-8 ON	F7	F7	DO Bus
Confirm	Bits 1-2 & 4-8 ON	FB	FB	DO Bus
Confirm	Bits 1 & 3-8 ON	Fd	Fd	DO Bus
Confirm	Bits 2-8 ON	FF	FF	DO Bus
Confirm	All Bits OFF	00	00	DO Bus

CALIBRATION CHART 017-1286-1

CAL. ADAPT. HEX DATA (POS. LOGIC) LOCATION U 2	U 1	TEST DESCRIPTION	STEP NO.	PROGRAMMER WORD COUNT DEC	HEX	OCT	SWITCH POSITIONS S2	S3	MEASUREMENT TEST PT.	ADJ.	LIMITS MIN	NOM	MAX
64	04	ADDRESS TEST A2 VIH	8-14	1365	555	2525	7	18	TP3		4.8		5.15
64	04	ADDRESS TEST A3 VIL	8-15	1365	555	2525	7	17	TP3		0.0		0.4
64	04	ADDRESS TEST A4 VIH	8-16	1365	555	2525	7	16	TP3		4.8		5.15
64	04	ADDRESS TEST A5 VIL	8-17	1365	555	2525	7	15	TP3		0.0		0.4
64	04	ADDRESS TEST A6 VIH	8-18	1365	555	2525	7	14	TP3		4.8		5.15
64	04	ADDRESS TEST A7 VIL	8-19	1365	555	2525	7	13	TP3		0.0		0.4
64	04	ADDRESS TEST A8 VIH	8-20	1365	555	2525	7	2	TP3		4.8		5.15
64	04	ADDRESS TEST A9 VIL	8-21	1365	555	2525	7	3	TP3		0.0		0.4
64	04	ADDRESS TEST A10 VIH	8-22	1365	555	2525	7	4	TP3		4.8		5.15
64	04	ADDRESS TEST V11 VIL	9-1	2047	7FF	3777	7	7	TP3		0.0		0.4
64	04	ADDRESS TEST V11 VIH	9-2	2048	800	4000	7	7	TP3		4.8		5.15
64	04	← DATA PATTERN FOR ALL WORDS NOT SHOWN											

at the address containing data and will STOP in FWD.

h. Press SKIP. The programmer will mis-verify at the address containing data and will halt in REV.

Revision "B" or later Software: Press the FWD key to set the programmer in FORWARD and the REV key to set it in REVERSE.

System 19: With KEYBD selected, press ENTER to set the programmer in FORWARD. Press ENTER and then REVIEW to set it in REVERSE.

4.3.4 LOAD DATA ONTO THE DI BUS

The data on the Calibration Chart is to be loaded on the DI bus using the programmer keyboard.

Models 1, 2 and 5: Key in binary data called out on the Calibration Chart. (Bits called out must be ON, bits not called out must be OFF.) Perform the necessary number-system conversions if using an octal or hexadecimal keyboard. Confirm correct data by checking the binary DI display.

Model 3: Use an external source, such as a paper tape reader, to put binary data on the DI bus.

Model 9: See MODEL 9 USERS NOTE, paragraph 4.3, to determine the correct revision letter.

Revision "A" Software: Halt the programmer in the automatic program mode with data on the DI bus.

a. Clear RAM: Select INVERT. Then press and hold the EDIT key while pressing LOAD.

b. Press the KEYBOARD key, and key in the Model 9 hex data called out on the Calibration Chart.

c. Press the PROGRAM key.

d. Ground J1-16 on the analog card.

e. Press EXECUTE and wait for the programmer to abort.

f. Press STOP, KEYBOARD and EXECUTE.

g. Disconnect J1-16 from ground.

h. SET the address specified on the Calibration Chart in order to make the measurement.

Revision "B" or later Software: With the EXECUTE indicator illuminated and all the others OFF, use the hex keypad to key in the Model 9 hex data called out on the Calibration Chart.

System 19:

a. Press KEYBD, key in the address and press ENTER.

b. Key the System 19 hex data into RAM at the specified address.

c. Press ENTER and then REVIEW.

4.3.5 CONFIRM DATA ON THE DO BUS

Models 1, 2, 3 and 5: Compare the bit callout on the Calibration Chart with the OUTPUT DATA display on the programmer front panel. Bits not called out must be OFF.

Model 9: With the EXECUTE light ON, press the PROM key and observe the data display on the programmer front panel. Data must match the hex callouts on the Calibration Chart.

System 19: With KEYBD selected, press the DEVICE DATA key. Hold it down while reading the hex data. The programmer must be in START.

4.4 WAVEFORM OBSERVATION

Programming waveforms should be observed after complete DC calibration of the programmer and Program Card Set. Set-up instructions assume that the calibration equipment is already installed for calibration per paragraph 4.2.

In waveform observation, oscilloscope displays are to be compared with the Timing Diagram. These waveforms, indicated by circled digits on the Timing Diagram, have the same reference on the Calibration Chart. Waveforms are selected using Universal Calibrator switches S2 and S3 as specified on the Calibration Chart.

4.4.1 CALIBRATION EQUIPMENT SET-UP

Refer to Figure 4-5.

a. Make sure that the programmer power is OFF.

b. Remove the digital card from the card slot.

c. Check the Timing Diagram to determine the number of the reject jumper. Find and remove the jumper on the digital card (if installed), making sure to note the position in which it is installed.

CAUTION

Be sure to replace the reject (abort) jumper (if it was installed) in the proper position after waveform observation.

d. Disconnect the 16-conductor cable at J1 of the Universal Calibrator.

e. Connect the free end of the 16-conductor cable to digital card J1, making sure that the red cable stripe and pin 1 are properly oriented.

f. Connect the triggered input of a dual-trace oscilloscope to the digital-card test point as indicated to the left of the TEST waveform on the Timing Diagram. Connect an input probe to TP3 on the calibrator.

g. Reinstall the digital card in the slot from which it was removed.

h. Ground J1-16 (Read Enable line) to the GND test point on the Universal Calibrator.

CAUTION

Do not connect J1-16 to any other potential; damage to programmer components may result.

4.4.2 TEST PROCEDURE

Observing programming waveforms requires putting data in RAM and causing the programmer to attempt to program a nonexistent device.

1. Turn programmer power ON.
2. Prepare the programmer for keyboard data entry.

Models 1—5, press:	RESET RAM-RAM PROGRAM MANUAL START
Model 9:	Set the NORMAL/INVERT switch in NORMAL. Press: KEYBOARD.
System 19 press:	KEYBD Ø ENTER

3. Key in data for bit 1 at several addresses:

Models 1—5:	Enter bit 1 at several addresses and confirm that bit 1 is ON and all other bits are OFF on the DI display.
Model 9:	Enter hex data "Ø1" at several addresses.
System 19:	Enter hex data "Ø1" at several addresses. Return to address Ø.

4. Select the PROGRAM mode:

Models 1 — 5, press:	RESET PROGRAL AUTO RAM-ROM2
Model 9, press:	PROGRAM
System 19, press:	SELECT C1 START PROG

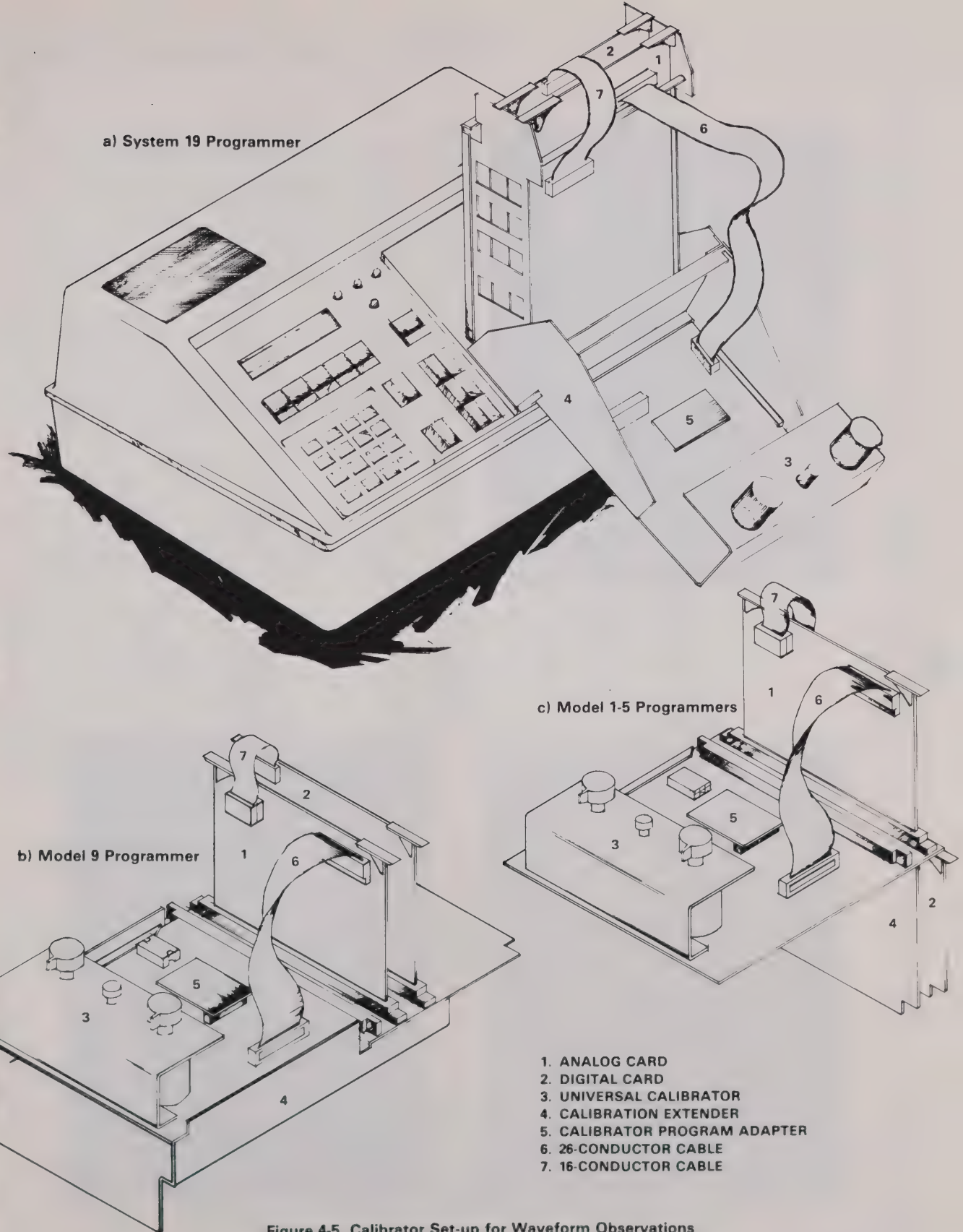
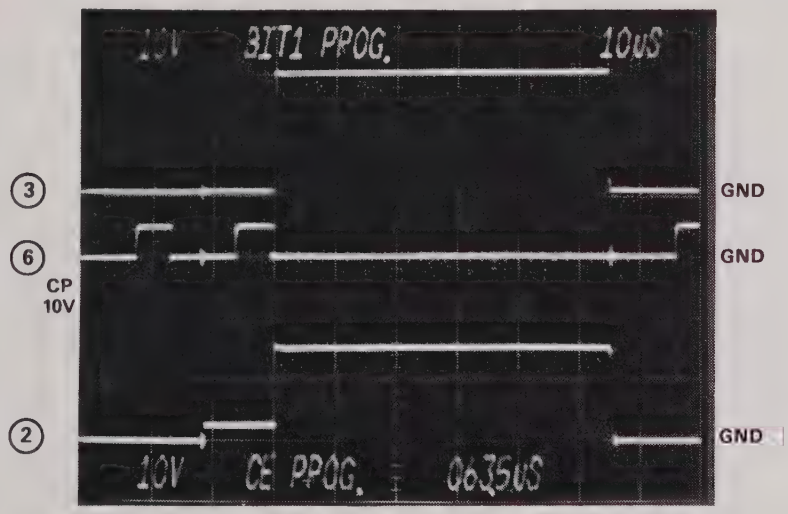
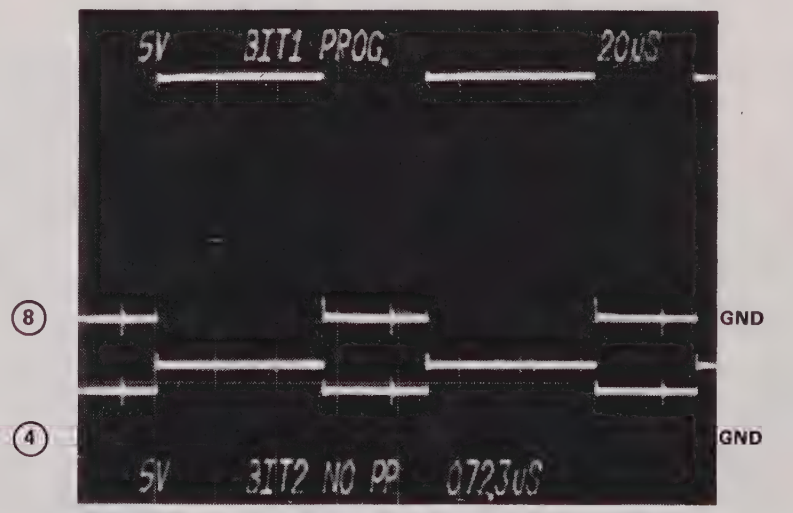


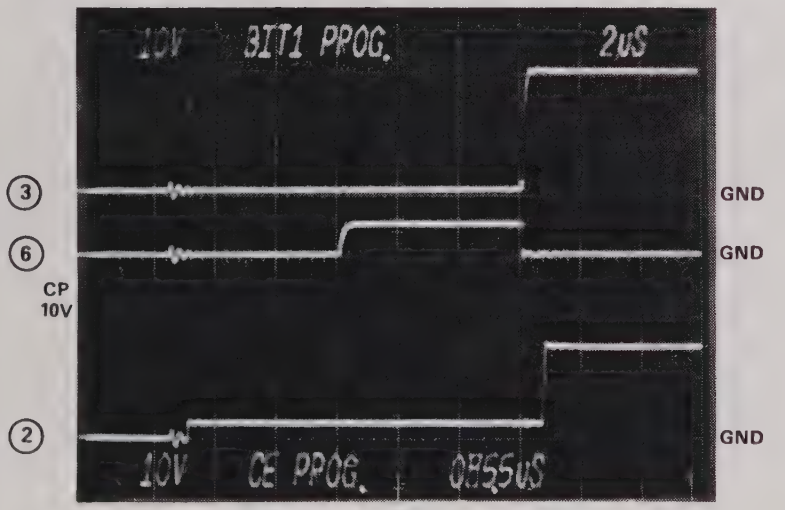
Figure 4-5. Calibrator Set-up for Waveform Observations


10V 3IT1 PROG. 10uS
3
GND
6
GND
CP
10V
2
GND
10V CE PROG. 0635uS

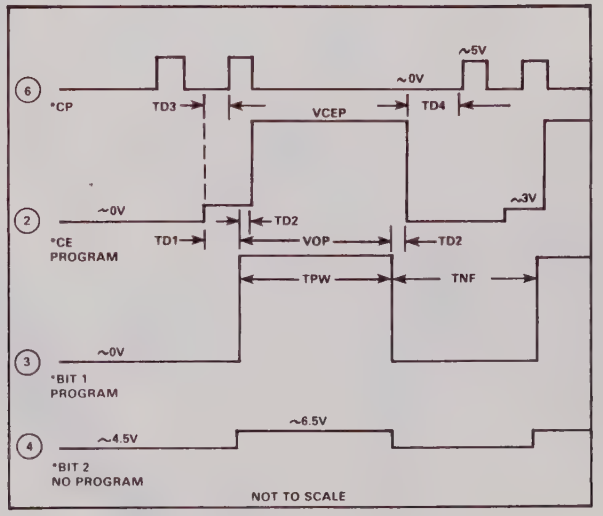
1


5V 3IT1 PROG. 20uS
8
GND
4
GND
5V 3IT2 NO PP 0723uS

3


10V 3IT1 PROG. 2uS
3
GND
6
GND
CP
10V
2
GND
10V CE PROG. 0855uS

2

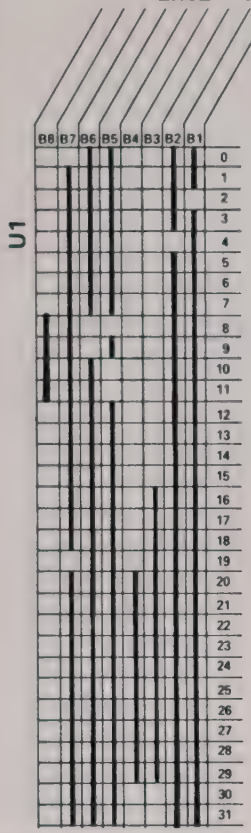

6
*CP
~5V
~0V
TD3
VCEP
TD4
2
~0V
~3V
TD2
*CE
PROGRAM
TD1
VOP
TD2
TPW
TNF
3
~0V
*BIT 1
PROGRAM
4
~4.5V
~6.5V
*BIT 2
NO PROGRAM
NOT TO SCALE

4

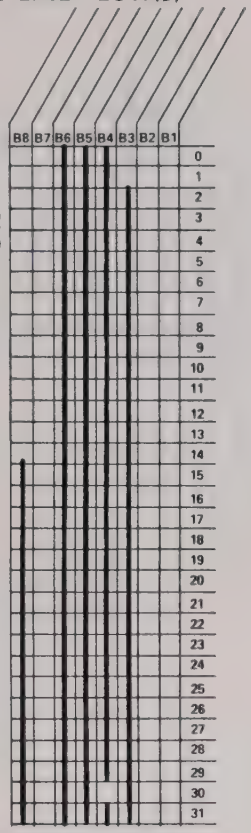
TRUTH TABLES

LINE = HI(1): NO LINE = LOW(Ø)

U1



U15



DIGITAL CARD JUMPERS

JP1	= OPEN
JP2	= SHORT
JP3	= SHORT
JP4	= SHORT
JP5	= SHORT
JP6	= SHORT
JP7C	= 29 PULSE REJ
JP7M	= NO PULSE REJ
JP8	= OPEN
JP9	= N
JP10	= 2048 (word limit)
JP11	= SHORT
JP12	= SHORT

WAVEFORM VARIABLES

VARIABLE	MIN	NOM	MAX	UNIT	COMMENTS
VCCP	5.00	5.25	5.50	V	
VCC VL	4.00	4.25	4.50	V	
VCC VH	4.75	5.00	5.25	V	
VCC READ	4.75	5.00	5.25	V	
VCEP	14.5	15.0	15.5	V	
VOP	21.5	20.0	20.5	V	
TD1	100			n sec	
TD2	100		1000	n sec	
TD3	1		7	u sec	
TNF			40	u sec	
TPW 1	50	55	60	u sec	FAST CLK
TPW 2	8.5	10	11.5	m sec	SLOW CLK
TD 4	5		15	u sec	

NOTES

1. *Oscilloscope trigger point: TP1 on the Digital Card, 701-1225. Trigger on the negative slope.*
2. **O** *These waveforms correspond to callouts on the calibration chart. Switch S2 and S3 of Universal Calibrator is indicated position, and depress S1 to obtain waveforms. Refer to Performance Check section of manual for detailed steps.*
3. *For calibration the card set polarity defaults to VOH.*
4. *Time and voltage bases, as well as any delay times, are printed on each photograph.*
5. ◄ *indicates a waveform section expanded to show detail. The expanded portion is shown in the second waveform of the same photograph. The time base of the delayed waveform is printed in the upper right portion of the photograph.*

REVISIONS

ZONE	LTR	DESCRIPTION	CM.	PE.	DATE
	H	ECN #4348	EF		12-81

DATA I/O ISSAQUAH, WA

TITLE: TIMING DIAGRAM	DRAWN BY: KT
	CHECKED BY: GL

SIZE	CODE IDENT. NO.	DRAWING NO.
B	54193	007-1286-1

SCALE | SHEET 1/1

5. Initiate waveforms:

Models 1 — 5, press:	START
Model 9, press:	EXECUTE
System 19, press:	START

After initiating the programming sequence, the programmer will halt at the first address which has data. Refer to the Timing Diagram and Calibration Chart by the circled digits (1 , 2 , 3 , ...). Make the indicated switch selections with S2 and S3 on the Universal Calibrator.

Observe specific waveforms relative to the triggered test pulse by pressing S1 on the calibrator. S3 is used to route analog card output to TP3 (the oscilloscope probe); S2 selects resistive loads that are applied when S1 is pressed. All other information on the Calibration Chart is of no importance during waveform observation.

CAUTION

When S1 is depressed, high currents are induced within the programmer; do not hold S1 depressed for extended periods.

6. Stop programming:

Models 1 — 5 and 9, press:	STOP
System 19, press	KEYBD

4.4.3 REJECT JUMPER REINSTALLATION AND ABORT TEST

Before putting the Program Card Set back in use, it is necessary to reinstall the reject (abort) jumper and confirm the operation of the abort function on the digital card.

CAUTION

The reject jumper must be reinstalled. Otherwise, the device's programming specifications will be violated, and the programmer and/or cardset may be damaged by a prolonged attempt to program a defective device.

1. Turn the programmer power OFF.
2. Remove the digital card from the card slot.
3. Refer to the Timing Diagram for the reject jumper number and make sure to install the jumper in the position from which it was removed.
4. Reinstall the digital card in the card slot.
5. Jumper the Read Enable line, digital card J1-16 to ground.
6. With the Universal Calibrator switches set to observe Bit-to-Program, connect an oscilloscope probe to TP3 on the calibrator trigger on TP3.
7. Repeat the key sequence in the Waveform Test Procedure, 4.4.2 steps 1-5.

Note with the oscilloscope that the waveform display is terminated. This indicates that the abort function of the digital card is operative. The System 19 will display ERR 22.

NOTE

The digital card has one or more potentiometers for calibrating various timing functions of the card set. In normal usage, the card set will rarely need to have these functions re-calibrated.

However, in the event that the card set waveforms do not conform to the specifications of the Timing Diagram contact your nearest Data I/O Service Representative for calibration information.

SECTION 5
CIRCUIT DESCRIPTION

5.1 INTRODUCTION

Data I/O Program Card Sets consist of a Digital Card, an Analog Card, and interconnecting cables. Both cards interface with the Programmer and with each other. The analog card interfaces with the PROM being programmed. Figure 5-1 gives a generalized block diagram of the relations between the cards, the Programmer, and the PROM being programmed or read.

5.1.1 DIGITAL CARD

The digital card receives data from the Programmer on the DI Bus, and from the PROM on the DO Bus. These data are compared at each bit of each PROM word both before and after programming. At each bit, the digital card continues to command PROM program pulses from the analog card until either ABORT or REJECT is signalled or until the bit is programmed.

5.1.2 ANALOG CARD

The analog card receives bit addresses, word addresses, timing, and mode commands. Analog card output consists of PROM manufacturers' specified programming voltages and currents. When specified by the manufacturer, each programmed PROM bit is tested for loading and/or leakage. Following the program cycle, PROMs are read by the analog card to verify that programmed data matches truth table data.

5.1.3 DETAILED CIRCUIT DESCRIPTION

The following paragraphs explain functional operation of the analog card and the digital card. Also included are discussions of signal flow, timing and reject conditions. Detailed circuit schematics are found at the rear of this manual — refer to these for pin-out and interconnection information.

5.2 DIGITAL CARD

Figure 5-2 gives a generalized block diagram of the digital card. This diagram shows signal flow and functional relationships between the blocks, but does not include detailed interconnect information. Refer to the schematics and timing diagram (with truth tables) for details of circuit connection and operation. The following paragraphs discuss the functions performed by the digital card.

5.2.1 SELECT GATES

U17 and U18 (on schematic) monitor Program Select (LL), Write Inhibit (PP), Read (X), and Read Inhibit (RR) in order to enable operation of the digital card. Output from Read Gate U17 is routed to the analog card to control the Data Bus Drivers. The Write Output Enable Gate allows the Program Memory to be set.

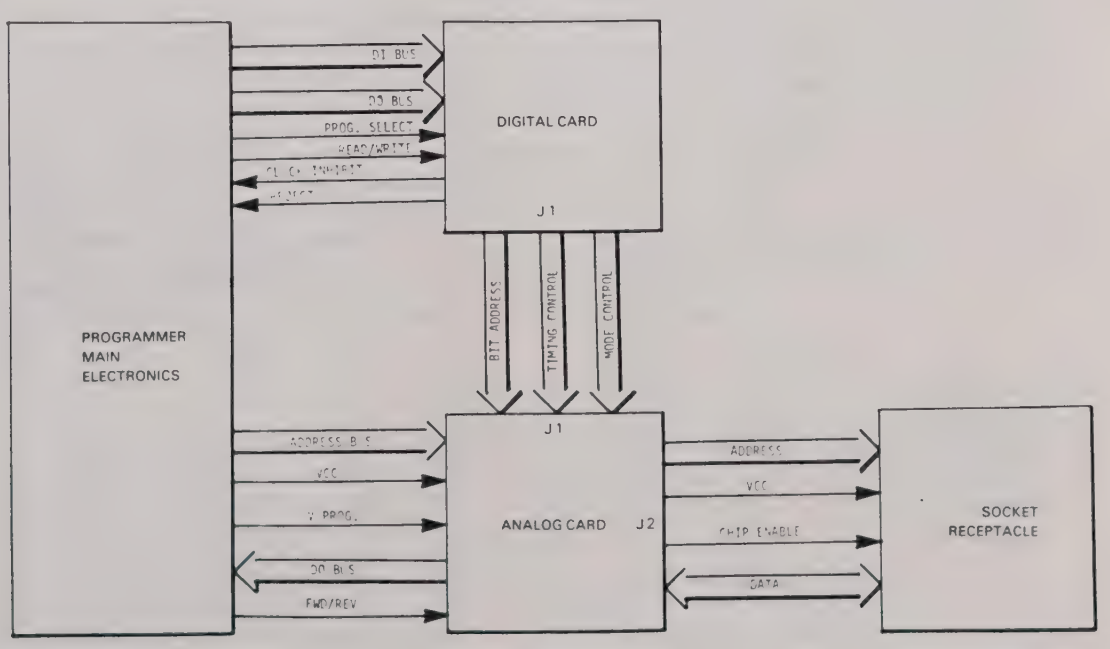


Figure 5-1. Simplified Block Diagram of Program Card Set

5.2.2 PROGRAM MEMORY

When the digital card is selected for operation, the Program Memory will set upon receiving a Write command on AA. This causes the Clock Generator on the digital card to begin operation and halts the programmer. Initialization of the Program Pulse Counter, Bit Counter and Sequence Counter and clearing of the Overprogram Counter occur before the Program Memory is set.

5.2.3 CLOCK GENERATOR

When the Program Memory sets in response to the Write and Program Select commands, the Clock Generator begins operation and the programmer is inhibited. Clock pulses increment the Sequence Generator. Alternate clock rates are determined by the Mode ROM or by the High Order (H/O) Memory (with JP8 connected). The Clock may be halted by the Abort Timer or by the Pause Timer (with CR2 connected).

5.2.4 SEQUENCE COUNTER

The 4-bit Sequence Counter drives the 32x8 Timing ROM. The combination generates timing signals for analog control, along with Bit Test and Bit Increment pulses, which are used on the digital card. (See the Timing Diagram.) A clock pulse is also output for PROMs with registers.

5.2.5 TIMING ROM

Output words from the Timing ROM are used in the serial Verify and Program operations, as shown in the Timing Diagram. Verify operations use Low Order words 0 to 15; Program operations use High Order words 16 through 31. Words 8 through 11 are used to output control signals for Vcc voltages during Read and Verify operations, which occur under machine control when the digital card is not selected. Those words are loaded through the Sequence Counter to the Timing ROM, as determined by the FWD line and Write Inhibit. (See the Schematic.)

At the beginning of a programming sequence (word 2), the Timing ROM outputs a Bit Test pulse to the Bit Test gate. If the DO Bus Decoder determines that there is no bit already programmed in the PROM, and if the DI Bus Decoder determines that there is a bit to program, then the Compare Gate outputs a Bit to Program pulse.

5.2.6 OVERPROGRAM COUNTER

The Bit to Program pulse loads the Overprogram Counter and also sets the Bit to Program Memory. This, in

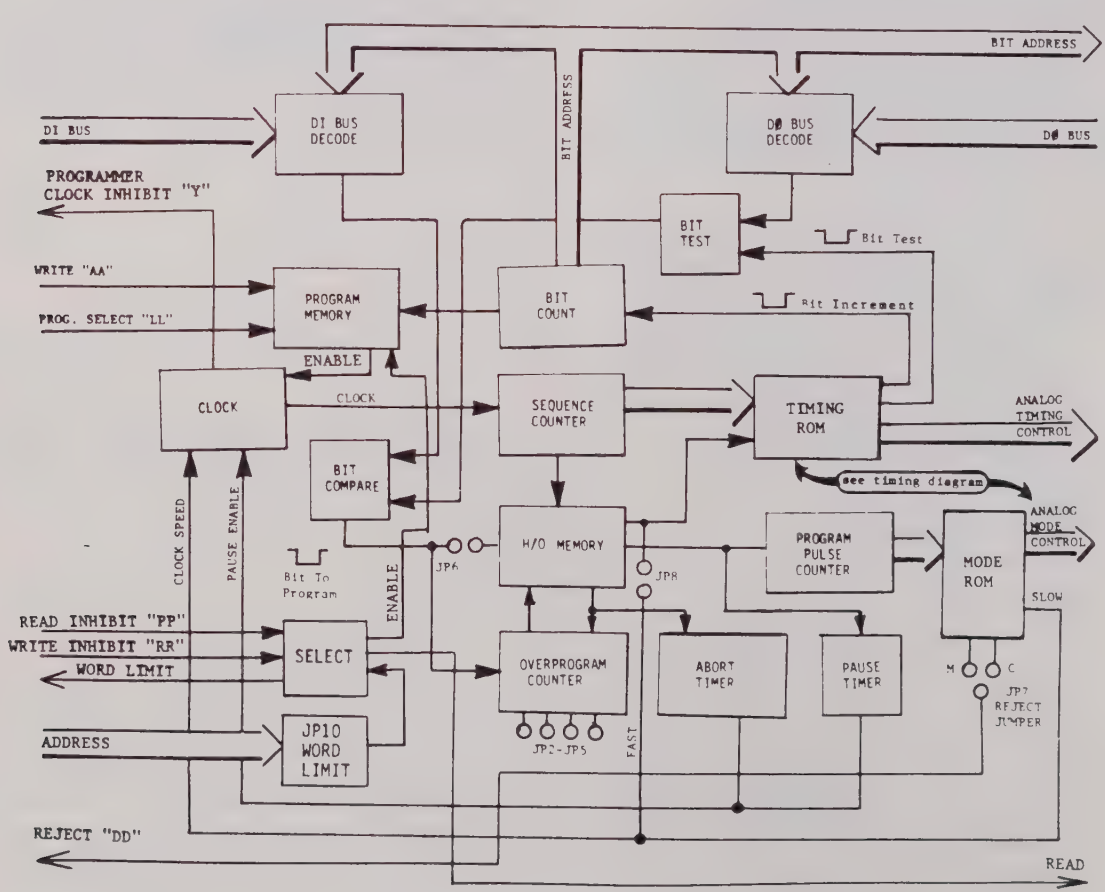


Figure 5-2. Block Diagram, 1225 Digital Card

turn, allows a carry pulse from the Sequence Counter to reach the high order memory. It also disables the Bit Count Gate until the Overprogram Counter clocks the Bit to Program Memory after the bit has been programmed.

At Timing ROM word 15, the carry pulse from the Sequence Counter toggles the H/O memory. This enables the fifth address line to the Timing ROM, and it advances into High Order (Program) Count, words 16 through 31.

At word count 31, the Sequence Counter outputs another carry pulse to again toggle the H/O memory. This sets the Timing ROM back to Low Order Count (Verify). At word 2, again, a Bit Test pulse is output from the Timing ROM; if the buses compare at Bit Test (bit is programmed), the output of the Bit Compare Gate remains unchanged (no Bit to Program), the H/O Memory remains enabled, and the Bit Count Gate remains disabled.

At word 15 the Sequence Counter outputs another carry pulse which again causes a High Order (Program) count, causing the Overprogram Counter to decrement. The above cycle repeats until the Overprogram Counter outputs a borrow pulse after counting down from the level preset by JP2—JP5. The borrow pulse resets the Bit to Program Memory which enables the Bit Count Gate, allowing it to decrement the bit count to the next bit.

Some 1225 cards are wired with JP6 shorted. With JP6 shorted, a Bit to Program pulse sets the High Order Memory. This causes the fifth address input line to the Timing ROM to go high, enabling the programming sequence of the Timing ROM. At word 31, the carry pulse from the Sequence Counter shifts the count sequence back to Low Order. With JP6 shorted, the total sequence is 16 pulses long.

5.2.7 PROGRAM PULSE COUNT AND MODE CONTROL

As program pulses are delivered to the PROM being programmed, the Program Pulse Counter counts up; outputs from the Program Pulse Counter are used as address line inputs to the Mode Control ROM. The Timing Diagram includes the truth table for the Mode Control ROM. Outputs of the Mode ROM control the magnitude of the program pulses (bits 1 and 2), along with clock speed (bit 3). Bits 4 and 5 control the number of programming attempts allowed before a reject is signalled to the programmer; reject jumper JP7 selects either the M line or the C line. (See the Timing Diagram for the pulse numbers selected.)

5.2.8 BIT COUNTER

The Bit Counter counts bit increment pulses arriving from the Timing ROM through the Bit Counter Gate. This gate is disabled, halting the Bit Counter, when the Bit to Programmer is set by a Bit-to-Program pulse. The Bit Counter counts down from either 4 or 8, as determined by the socket adapter or the Mode ROM. Output from the Bit Counter controls the DO Bus Decoder and DI Bus Decoder as well as the Bit Decoder on the Analog Card. When the Bit Counter reaches zero, its borrow output is used to reset the Program Memory.

5.2.9 ABORT TIMER

The Abort Timer measures the time required to program a bit. If programming time is excessive, and JP1 is shorted, a REJECT is signaled and the clock is halted. The Abort Timer is connected to the Overprogram Counter such that an abort is possible only during Low Order Count (Verify cycle). Some card sets don't use this function.

5.2.10 PAUSE TIMER

Some card sets use the Pause Timer to measure the time to program the PROM. A transistor is used in conjunction with the timing components to integrate out the time that the Program Memory is set. If programming time exceeds the value set by circuit components, the Clock is stopped in order to allow the PROM to cool; after a pause in the order of seconds the Clock is allowed to start again, and programming continues. The Pause Timer output is gated with the Timing ROM so that a pause cannot occur during program pulses.

5.2.11 WORD LIMIT SELECT

Word Limit is jumper-selected at JP10 on the digital card. JP10 limits the address range of the programmer through the Word Limit line (CC), according to the configuration of the PROM being programmed. Selection defaults to the socket adapter.

5.3 ANALOG CARD

The 1286-1 analog card provides the drive information, sense amplifiers and power supplies required to program AMD generic-family PROMs, as commanded by signals from 1225 digital card.

Figure 5-3 shows signal flow between analog card components and the PROM being programmed. Refer to the truth tables on the timing diagram for precise details about signal amplituteds and timing.

5.3.1 ADDRESS BUFFERS

Each address line from the Address Bus if buffered by a high voltage open-collector device (U13, U14) and applied to the appropriate device pin through J2.

5.3.2 Vcc SUPPLY

The Vcc Supply consists of an IC voltage regulator, U5, and pass-transistor Q10. The supply is killed during Stop by the action of the Start line, pin 22 on the edge connector. The various voltage levels during Read, Verify and Program are controlled via ROM U2. This ROM also controls loading of the PROM Bit Lines and controls the comparator reference level.

5.3.3 PROGRAM PULSE SUPPLY

The Program Supply consists of a Darlington emitter follower (Q14 and Q15) controlled by pin 4 of U3. U9 operates as an adjustable voltage clamp. When U9 goes high the base circuit capacitor of Q15 is charged from the +Prog supply, then clamped at the required voltage by U9

to provide a fast rise time. Gate U3, pins 5 and 6, is included to provide a fast fall time. The reference voltage for U9 is obtained from pin 6 of U5. Zener diode CR16 and transistor Q13 perform the current-limit function.

5.3.4 CHIP ENABLE PULSE SUPPLY

The Chip Enable Supply consists of emitter follower, Q1, controlled by Pin 2 of U3. As in the Program Pulse supply, a voltage clamp (U8) is used to provide a fast rise time. Diode CR1 allows the CE to have three states: 0 V; +5 V, supplied by pull-up R33; and +15 V, supplied by Q1.

5.3.5 BIT DECODER

The Bit Decoder, U4, receives its input from the Bit Counter on the digital card. The state of pin 12 of U4 controls the state of the particular output selected by the other three input lines.

5.3.6 PROGRAM SWITCH

The Program Switch consists of eight transistor switches Q2-Q9 connecting the Program Pulse Supply to the various device bit outputs and driven from the Bit Decoder. The selected bit-to-program is connected to the Program Pulse Supply voltage. Unselected bits are held low during the program pulse.

5.3.7 DATA COMPARATORS

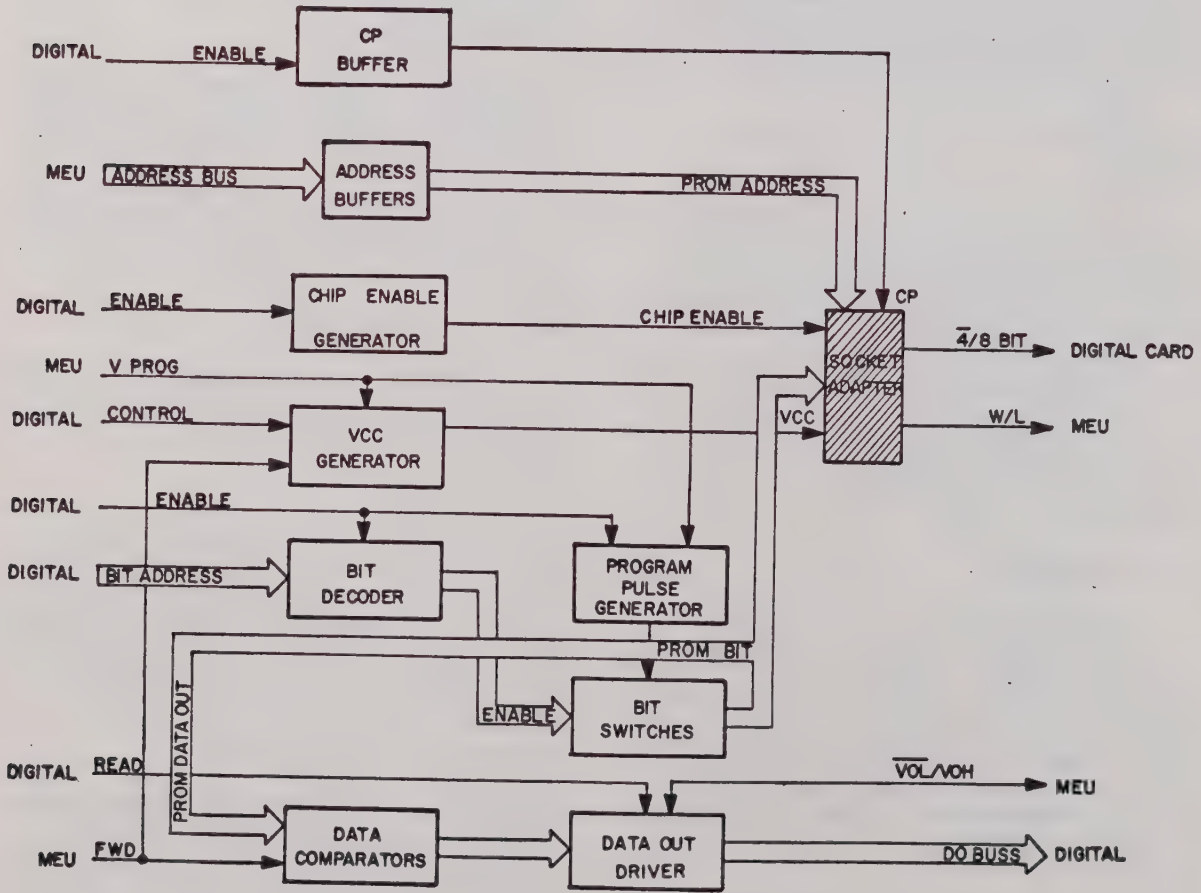
The bit lines from the device are connected to the non-inverting inputs of the comparators, U6 and U7. The inverting input is connected to a voltage reference source. Thus the variable compare level allows parametric testing of VOL and VOH devices.

5.3.8 DATA BUS DRIVERS

The output of the comparators is fed to Data Bus Drivers U11 and U12. The Data Bus Drivers are gated by a common line from the Digital Card so that device data is presented to the Bus at the correct time. The drivers invert the data on command from the socket adapter via pin 7 of J2. This allows for automatic data inversion for VOL or VOH devices.

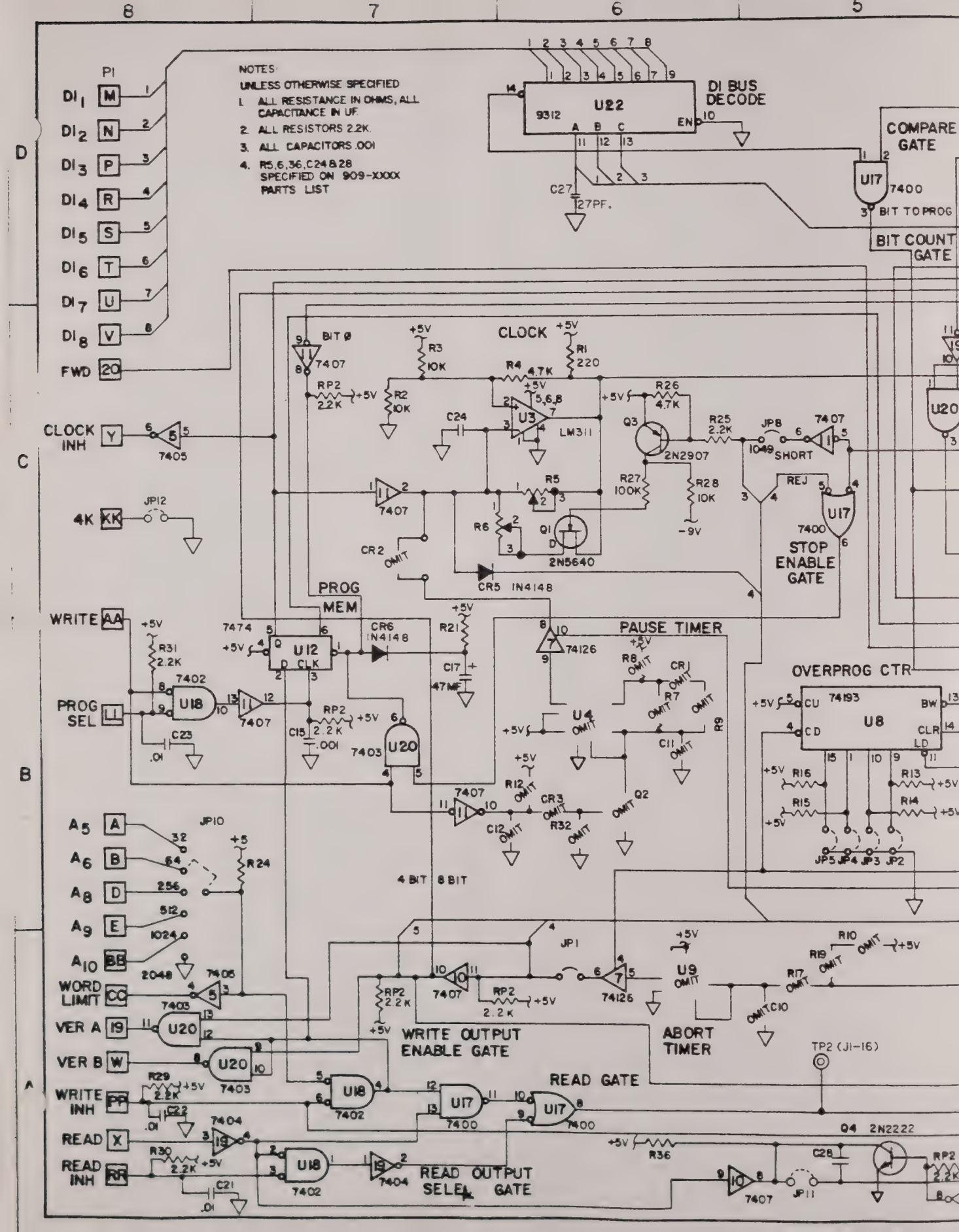
5.3.9 CP GENERATOR

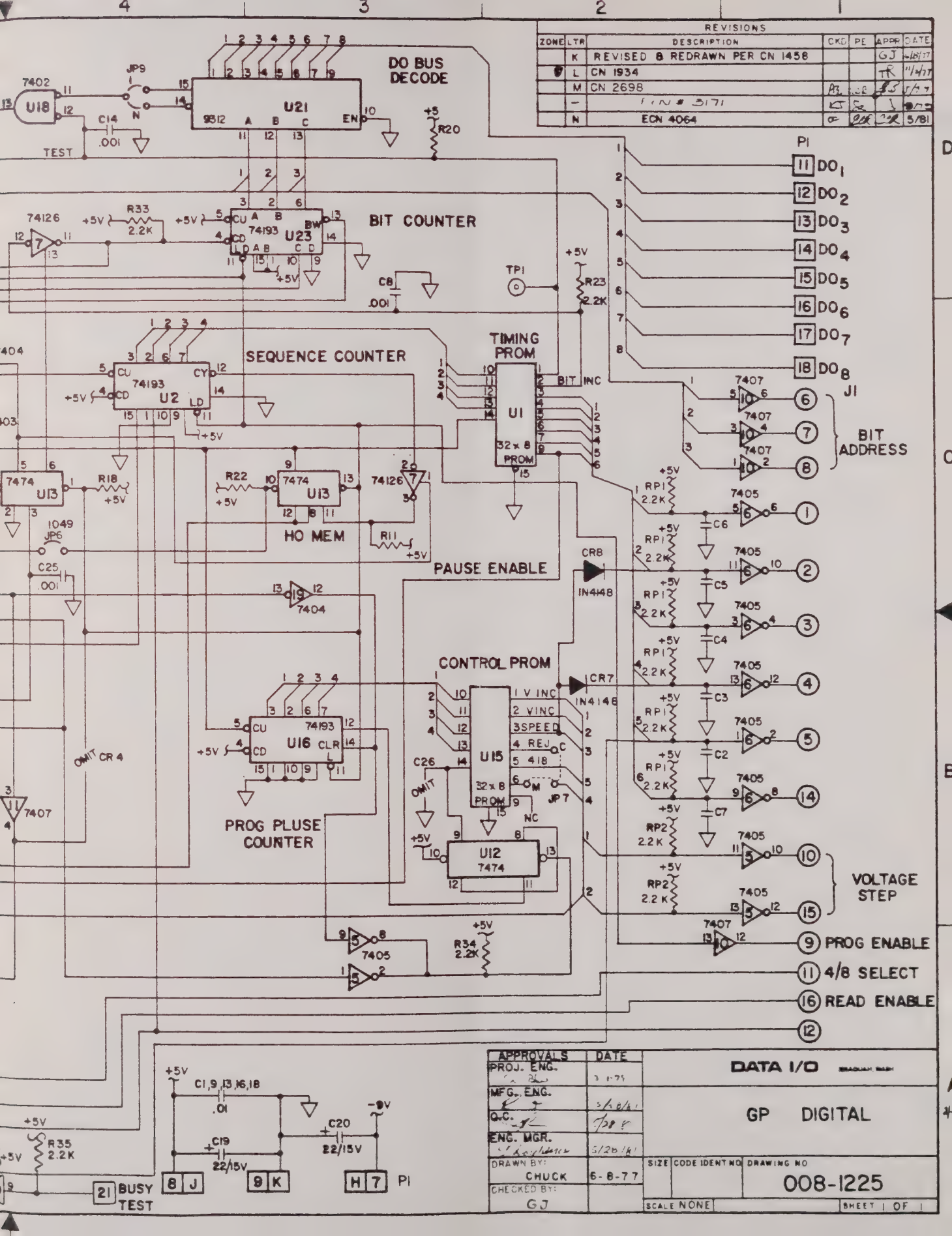
The Clock Pulse (CP) Generator consists of pins 8 and 9 of U1, controlled by J1-5. Output from the generator is applied to the appropriate device pins through J2. This provides the necessary clocking required on PROM devices incorporating registers or latches.

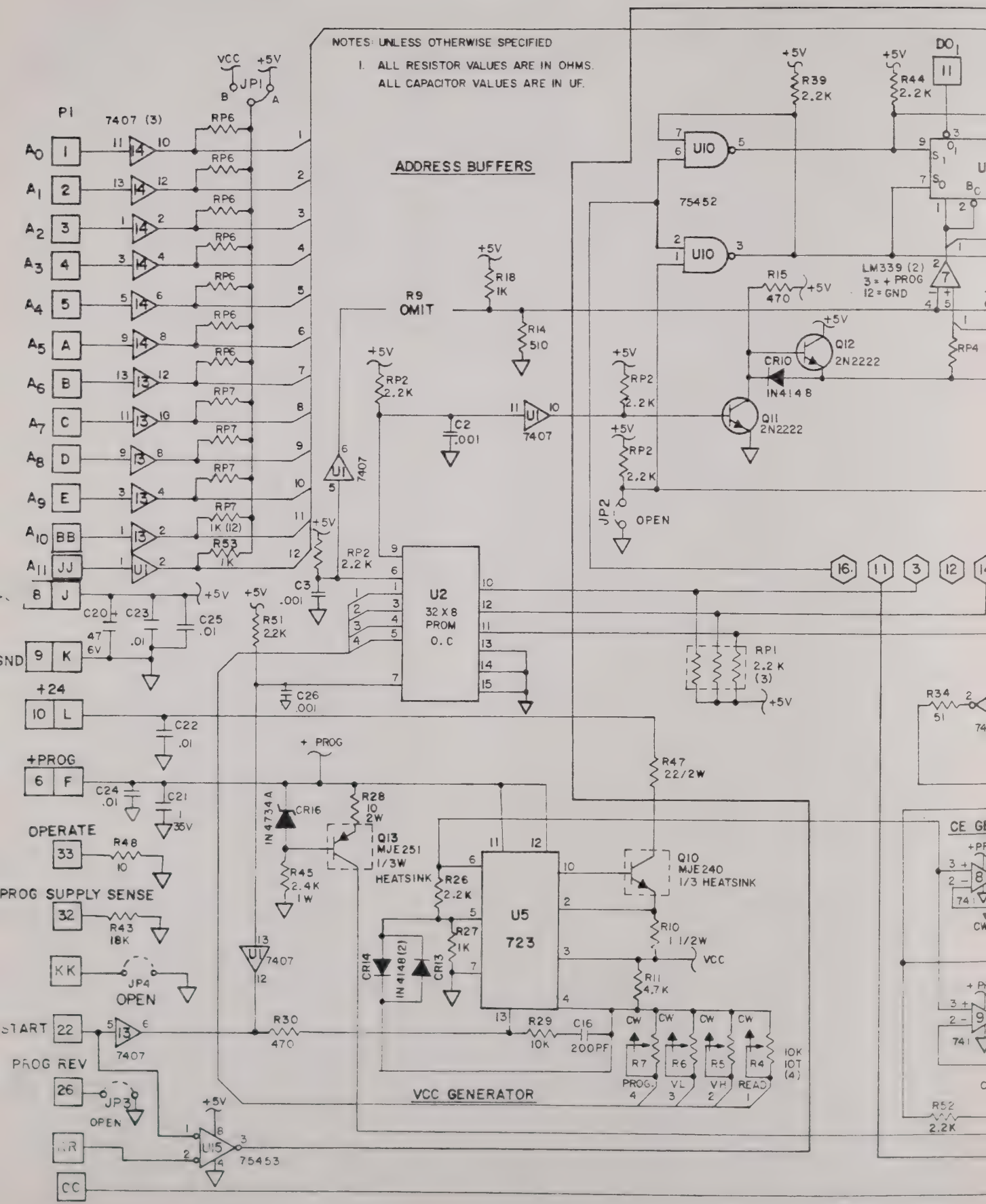


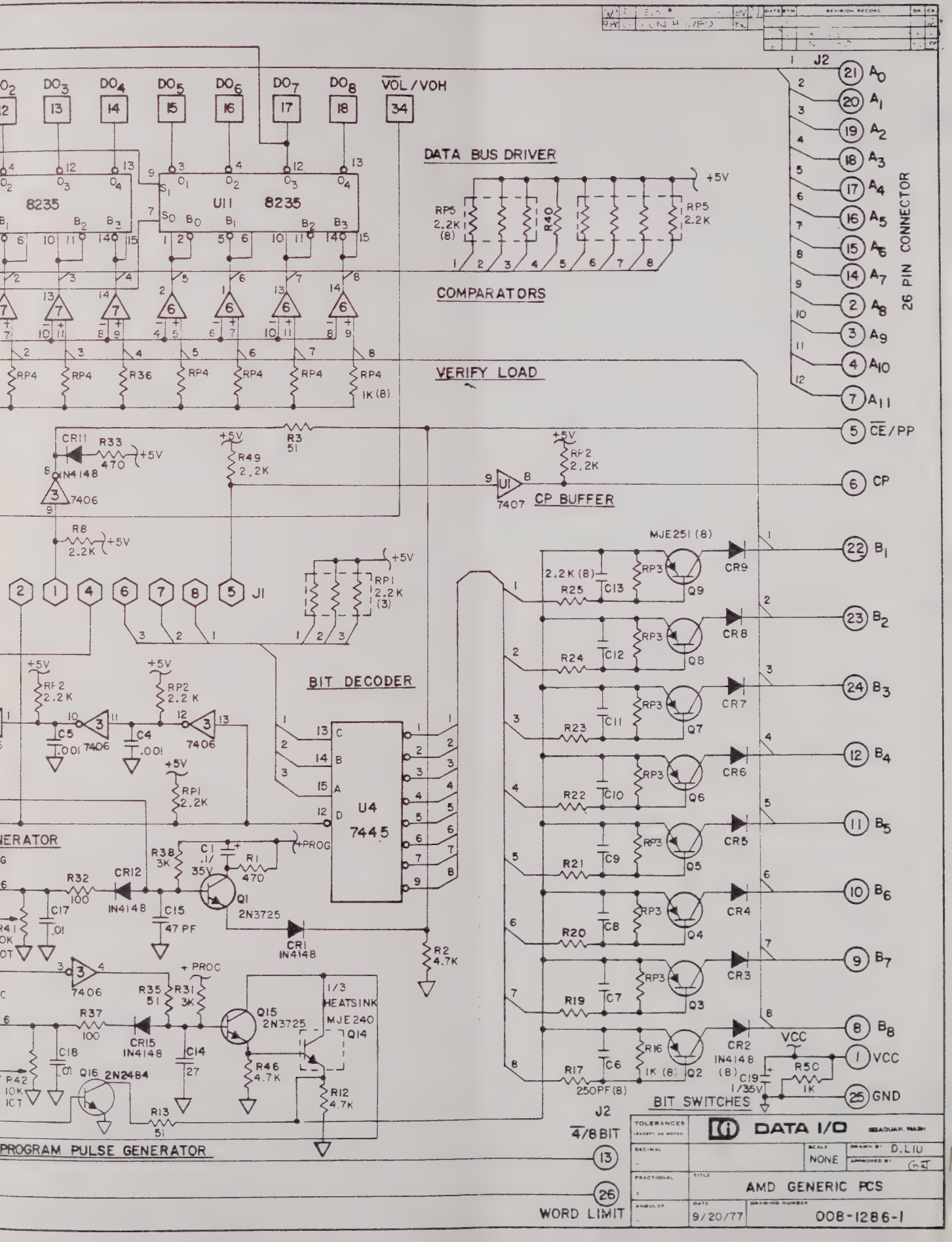
SECTION 6
SCHEMATICS

008-1225	GP Digital
008-1286-1	AMD Generic Analog
010-1286-1	Truth Table
008-1072	Calibration Adapter

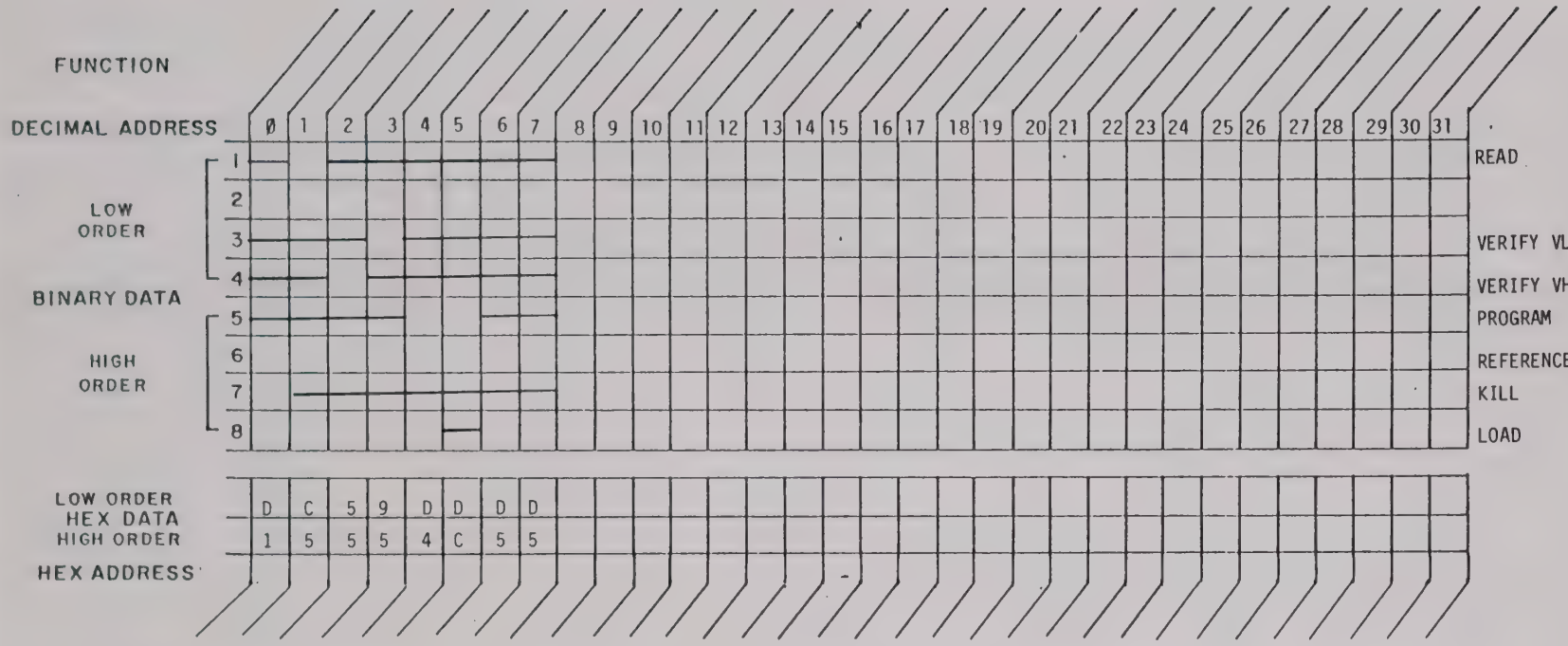

NOTES:
UNLESS OTHERWISE SPECIFIED
1. ALL RESISTANCE IN OHMS, ALL CAPACITANCE IN UF.
2. ALL RESISTORS 2.2K.
3. ALL CAPACITORS .001
4. R5,6,36,C24&28 SPECIFIED ON 909-XXXX PARTS LIST
P1
DI1 M
DI2 N
DI3 P
DI4 R
DI5 S
DI6 T
DI7 U
DI8 V
FWD 20
CLOCK INH Y
4K KK
WRITE AA
PROG SEL LL
A5 A
A6 B
A8 D
A9 E
A10 BB
WORD LIMIT CC
VER A 19
VER B W
WRITE INH PP
READ X
READ INH RR
U22 9312
DI BUS DECODE
C27 27PF.
COMPARE GATE
U17 7400
BIT TO PROG
BIT COUNT GATE
BIT Ø
7407
CLOCK
R3 10K
R1 220
R4 4.7K
RP2 2.2K
R2 10K
U3 LM311
C24
R26 4.7K
Q3 2N2907
R25 2.2K
JP8 1049 SHORT
R27 100K
R28 10K
-9V
REJ
STOP ENABLE GATE
R5
R6
Q1 2N5640
CR2 OMIT
CR5 IN4148
PROG MEM
7474
U12
CR6 IN4148
R21
C17 47MF
PAUSE TIMER
74126
R8 OMIT
CR1 OMIT
R7 OMIT
C11 OMIT
R9
U4 OMIT
OVERPROG CTR
74193
U8
R16
R15
R13
R14
JP5 JP4 JP3 JP2
R31 2.2K
7402
U18
C23 .01
7403
U20
C15 .001
R12 OMIT
CR3 OMIT
Q2 OMIT
R32 OMIT
C12 OMIT
JP10
R24
4 BIT 8 BIT
JP1
U9 OMIT
R10 OMIT
R18 OMIT
R17 OMIT
C10 OMIT
WRITE OUTPUT ENABLE GATE
ABORT TIMER
TP2 (J1-16)
READ GATE
R29 2.2K
C22 .01
7404
R30 2.2K
C21 .01
READ OUTPUT SELECT GATE
Q4 2N2222
R36
C28
JP11


REVISIONS
ZONE LTR DESCRIPTION CKD PE APPR DATE
K REVISED & REDRAWN PER CN 1458 GJ 6/8/77
L CN 1934 TR 11/4/77
M CN 2698 5/8/78
- P/N # 3171
N ECN 4064 5/81
DO BUS DECODE
U21
9312
BIT COUNTER
U23
74193
SEQUENCE COUNTER
U2
TIMING PROM
U1
32 x 8 PROM
BIT INC
HO MEM
U13
7474
PAUSE ENABLE
CR8
IN4148
CONTROL PROM
U15
CR7
PROG PLUSE COUNTER
U16
CLR
OMIT CR 4
OMIT
C26
U12
NC
JP7
JP6
JP9
TEST
TP1
+5V
R20
R33
2.2K
R23
R22
R18
R11
C14
.001
C8
C25
1049
RP1
RP2
C6
C5
C4
C3
C2
C7
7407
7405
7404
7402
7403
7414
7426
J1
BIT ADDRESS
VOLTAGE STEP
P1
DO1
DO2
DO3
DO4
DO5
DO6
DO7
DO8
PROG ENABLE
4/8 SELECT
READ ENABLE
BUSY TEST
C1,9,13,16,18
.01
C19
22/15V
C20
-9V
R35
2.2K
8 J
9 K
H 7
APPROVALS DATE
PROJ. ENG.
MFG. ENG.
Q.C.
ENG. MGR.
DRAWN BY: CHUCK 6-8-77
CHECKED BY: GJ
DATA I/O
GP DIGITAL
SIZE CODE IDENT NO DRAWING NO
008-1225
SCALE NONE
SHEET 1 OF 1


NOTES: UNLESS OTHERWISE SPECIFIED
1. ALL RESISTOR VALUES ARE IN OHMS.
ALL CAPACITOR VALUES ARE IN UF.
ADDRESS BUFFERS
VCC GENERATOR
P1
7407 (3)
JP1
JP2
JP3
JP4
OPEN
R9 OMIT
U2
32 X 8
PROM
O. C
U5
723
U10
75452
U11
75453
LM339 (2)
3 = + PROG
12 = GND
Q10
MJE240
1/3 HEATSINK
Q11
2N2222
Q12
2N2222
Q13
MJE251
1/3W
HEATSINK
CR10
IN4148
CR13
IN4148 (2)
CR14
CR16
IN4734A
RP1
2.2 K
(3)
RP2
2.2K
RP4
RP6
RP7
R4
R5
R6
R7
10K
10T
(4)
PROG.
VL
VH
READ
OPERATE
PROG SUPPLY SENSE
PROG REV
START
+PROG
+24
+5V
VCC
GND


DO2 DO3 DO4 DO5 DO6 DO7 DO8 VOL/VOH
8235 U11 8235
DATA BUS DRIVER
RP5 2.2K (8)
R40
RP5 2.2K
+5V
COMPARATORS
VERIFY LOAD
RP4 RP4 R36 RP4 RP4 RP4 RP4 1K (8)
J2
26 PIN CONNECTOR
A0 A1 A2 A3 A4 A5 A6 A7 A8 A9 A10 A11
CE/PP
CP
CR11 R33 470 IN4148
R49 2.2K
R3 51
RP2 2.2K
U1 7407 CP BUFFER
7406
R8 2.2K
J1
RP1 2.2K (3)
BIT DECODER
U4 7445
RP2 2.2K
C5 .001
C4 .001
RP1 2.2K
+PROG
R38 3K
C1 .1/ 35V
R1 470
R32 100
CR12 IN4148
Q1 2N3725
C17 .01
C15 47 PF
CR1 IN4148
R2 4.7K
+ PROC
R35 51
R31 3K
Q15 2N3725
1/3 HEATSINK
MJE 240 Q14
R37 100
CR15 IN4148
C18 .01
C14 27
Q16 2N2484
R46 4.7K
R12 4.7K
R13 51
PROGRAM PULSE GENERATOR
MJE251 (8)
2.2K (8)
R25 C13 RP3 Q9 CR9
R24 C12 RP3 Q8 CR8
R23 C11 RP3 Q7 CR7
R22 C10 RP3 Q6 CR6
R21 C9 RP3 Q5 CR5
R20 C8 RP3 Q4 CR4
R19 C7 RP3 Q3 CR3
R17 250PF (8) C6 R16 1K (8) Q2 CR2 IN4148 (8)
B1 B2 B3 B4 B5 B6 B7 B8
VCC
R50 1K
C19 1/35V
VCC GND
BIT SWITCHES
J2
4/8 BIT
WORD LIMIT
DATA I/O
D.LIU
NONE
AMD GENERIC PCS
9/20/77
008-1286-1

DATE	RVH	REVISION RECORD	DR	CK
11-4-77	C	RELEASE	PW	GT



NOTES

1. "1" = HIGH.
2. "1" = PAPER TAPE HOLE.
3. FOR V_{OL} PROGRAMMING PROMS, INVERT SWITCH ON READER DRIVER CARD MUST BE INVERT.
4. ALL UNDEFINED ADDRESS LOCATIONS MUST BE ALL "1's", (HIGHS).

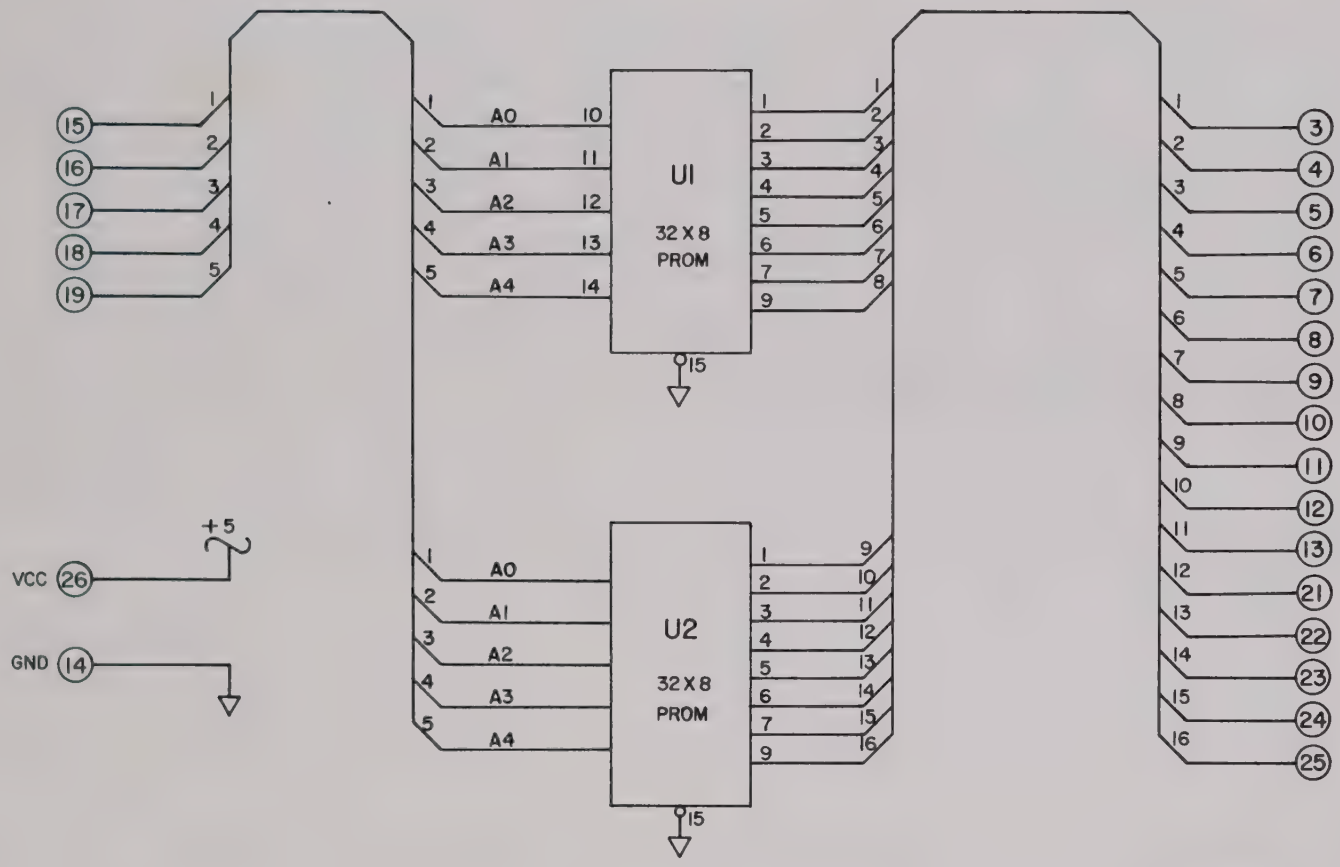
PROM LABEL

2-1286-1

"U" LOCATION
CARD NUMBER
DASH AND REVISION

TOLERANCES (EXCEPT AS NOTED)	DATA I/O ISSAQUAH, WASH.			
DECIMAL .	TRUTH TABLE	SCALE NONE	DRAWN BY WALTER	
FRACTIONAL .	TITLE AMD GENERIC PCS		APPROVED BY GT	
ANGULAR .	DATE 11-4-77	DRAWING NUMBER 010 – 1286-1	SHT 1/1	

DATE	SYM	REVISION RECORD	DR	CK
11-13-75	A	RELEASE		



TOLERANCES (EXCEPT AS NOTED)	DATA I/O ISSAQUAH, WASH.		
DECIMAL -		SCALE	DRAWN BY G. ROPPE
			APPROVED BY
FRACTIONAL -	TITLE PLUG IN ADAPTER (UNIVERSAL CALIBRATOR)		
ANGULAR -	DATE 10-15-75	DRAWING NUMBER 008-1072	

Reader Comments

The manual's completeness, accuracy, organization, usability, and reliability: _____

_____

Did you find errors in this manual? _____

How can this manual be improved? _____

_____

_____

Additional comments: _____

_____

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Company _____

Address _____

City _____ State _____ Zip _____ Phone _____

Manual or Part No. _____

0299/DEC 81

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Did this equipment arrive intact, without loose parts or cable damage? ☐ YES ☐ NO

Did the equipment operate on power-up? ☐ YES ☐ NO

Did you attain adequate system performance? ☐ YES ☐ NO

Were any electrical adjustments required? ☐ YES ☐ NO

If you required assistance, was a local Data I/O representative contacted? ☐ YES ☐ NO

Comments: _____

_____

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Department _____ M/S _____

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Address _____

City _____ State _____ Zip _____ Phone ( ) _____

Model or Description _____ Serial or Part No. _____

Date Received _____

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(b) Exclusive Warranty — The warranty set forth herein is the only warranty, oral or written made by Data I/O and is in lieu of and replaces all other warranties, expressed or implied, including the WARRANTY OF MERCHANTABILITY AND THE WARRANTY OF FITNESS FOR A PARTICULAR PURPOSE.

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Redmond, WA 98052

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NECESSARY
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IN THE
UNITED STATES

BUSINESS REPLY MAIL
FIRST CLASS PERMIT NO. 41 REDMOND, WA 98052

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Warranty/Registration
Service Manager
10525 Willows Road N.E.
C-46
Redmond, WA 98052

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